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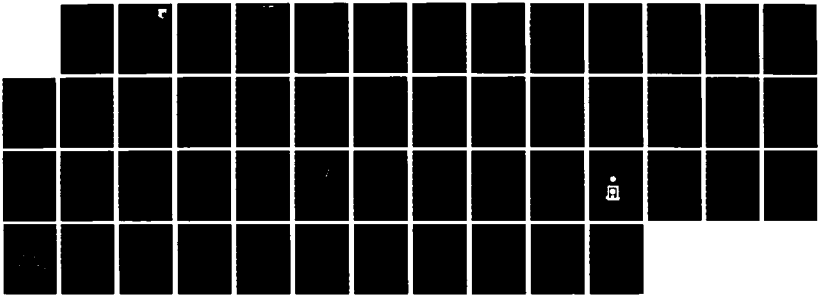

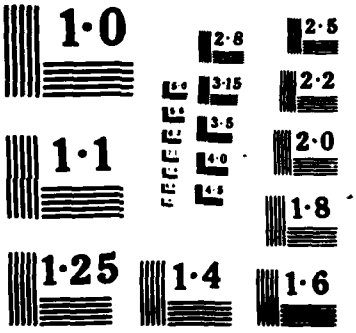
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HIGH EFFICIENCY MULTIPLE BANDGAP SOLAR CELL RESEARCH

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This technical report has been reviewed and is approved for publication.

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The objective of this 14-month effort was the development of GaAsP/GaP devices for stacking on silicon bottom cells to achieve high conversion efficiencies. The estimated efficiency of the completed devices was 21% AMO under concentrated light. A four-terminal stack was incorporated to allow voltage matching wiring schemes to account for differing degradation of the individual devices in the space environment. Device optimization was defined for a bandgap difference of 0.6 to 0.8 eV, with projected efficiencies of 27% for GaAsP/GaP stacked onto GaAsSb or GaInAs, and GaAs on Ge or GaSb.

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SUMMARY

Following redirection of this effort to focus on mechanically stacked cells in the eighth month of this 14-month contract, the first large area, stackable GaAsP solar cells have been formed on GaP substrates. They have respectable values for open circuit voltage and fill factor and their fabrication involved the simultaneous solution of seven challenging problems ranging from two surface grid alignment to the use of the thermal cracker. The highest performance was obtained with a small area $GaAs_{.7}P_{.3}$/GaP with an AM0 efficiency of 13.6% and a large area silicon cell of 7.1% AM0 efficiency as measured in a simulated mechanical stack under concentrated light. Combined, these provide an estimated 21% AM0 performance for this two-junction stack. A packaging scheme was developed to remove heat from the edges of the GaP wafer and allow the use of an adhesive between the two junctions that is thick enough to absorb the thermal stresses and to provide adequate standoff voltages. The specific contact resistance to the GaP was reduced to the 10^{-4} ohm-cm^2 level which allows operation at several hundreds-of-suns light intensities. A voltage matching wiring scheme was devised to provide superior end-of-life performance of two-junction solar cells in space. A band gap difference of 0.6-0.8 eV between the top and bottom junctions was identified as central to achieving maximum two junction performance. The projected practical efficiencies were calculated for mechancially stacked, two-junction devices. These values exceed 27% AM0 for $GaAs_{.7}P_{.3}$/GaP stacked onto 1.1 eV band gap GaAsSb or GaInAs and for GaAs stacked on Ge or GaSb.

Acknowledgment

Work on the low contact resistance to GaP, the cell processing and layer growths, were performed by M. S. Kuryla, R. E. Weiss, and R. A. Ransom.

HIGH EFFICIENCY MULTIPLE
BAND GAP SOLAR CELL RESEARCH

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I. Introduction

A. Background

The original objective of this 14-month contract was the achievement of high efficiencies by means of monolithic multiple junctions. In the course of this study, we found convincing evidence that the shortest and surest path to high efficiencies is with a four-terminal mechanical stack. With AFWAL's concurrence, the effort was redirected to four-terminal mechanical stacks during the eighth contract month. In the fourteenth contract month, the deliverables were modified at AFWAL's request, to add large area, stackable GaAsP/GaP solar cells.

Multiple junction solar cells with differing band gaps have the potential for much higher efficiencies than can be achieved with single-junction devices. Going from one to two junctions raises the theoretical efficiency limit by about one third.[1] Monolithic stacks, where two junctions are grown sequentially onto a single substrate, are conceptually very elegant. So far these monolithic structures have achieved efficiencies that are less than that of the best single-junction devices.[2-4] The problem is to provide adequate transition layers between the monolithic junctions while maintaining high performance in each junction with sufficient yield to give a complete structure of high efficiency. A simpler, faster, and more direct route is to form the two junctions separately and mechanically stack one on top of the other. Each junction can then be fabricated without interferences and then individually selected for high performance. This greatly increases yield. One approach to mechanically stacked cells is to use AlGaAs cells grown on GaAs substrates. The opaque GaAs is etched off and the thin AlGaAs is stacked on a Si bottom cell. So far this process has not given high efficiency top cells with the open gridded back contact required for stacking.[5,6] It is a distinct advantage to be able to process and mount the top cell using a thick and less fragile substrate. The latter is possible by the use of a transparent GaP wafer. A $GaAs_{.7}P_{.3}$ cell is grown on it, as shown in Figure 1. These materials and structure parallel that of the highly developed light-emitting-diode technology.

B. Accomplishments

The first, mechanically stackable, large area (0.317 cm^2) $GaAs_{.7}P_{.3}$ cells have been fabricated onto thick (300 micron) GaP substrates. The open circuit voltages of 1.0 V and fill factors of 0.7 have been obtained and peak quantum yields between 25-35% have

been achieved. The performance limiting parameters have been measured and the means for further improvement have been identified. These stackable cells were made possible by the simulataeous incorporation of solutions to seven challenging problems. These problems are: (1) the heat transfer problem for growth on free standing wafers solved with free moly blocks, (2) the low incorporation of P in layer growths circumvented with the thermal cracker, (3) the high, free carrier absorption of sub-band-gap photons in the GaP wafer corrected with low doped substrates, (4) the high contact resistance to low doped GaP reduced with a multilayer metalization and anneal, (5) the design and production of adequate grid masks accomplished with a computer optimization and with new mask fabrication, (6) the alignment of the frontside and backside grids facilitated with alignment marks at the transparent edges of the GaP wafer, and (7) the difficulty in processing both sides of a wafer without damage accommodated with a sequence of protective layers.

The highest performance was obtained with a small area (0.0386 cm^2) GaAsP junction formed on a GaP wafer and with a large area (0.317 cm^2) Si cell. Separate measurement of these devices provided an estimated stack efficiency of 21% AM0 for the 25-50X concentrated light range. Of this total, 13.6% was contributed by the GaAsP/GaP and 7.1% came from the bottom Si device. A configuration has been devised so that most of the heat generated in the top device can be conducted through the edges of the thick GaP wafer without the need to pass the heat through the bottom device. This allows an adhesive to be used to bond the top and bottom devices that is thick enough to absorb the thermal expansion mismatches and provide adequate voltage standoff between the top and bottom cells. The silcone adhesive, RTV-615, was identified as adequate for this task. A voltage matching wiring scheme was developed that reduces the end of life power losses due to radiation induced changes in current output from the top and bottom cells in a two-junction stack. The potential performance of mechanical stacks was evaluated in general. These projected efficiencies exceed 27% AM0 for $GaAs_{.7}P_{.3}$/GaP stacked onto 1.1 eV band gap GaAsSb or GaInAs and for GaAs stacked on Ge or GaSb when operated under 50-100X AM0 concentration ratios.

The devices of this study were grown with a new technique called Vacuum-Chemical-Epitaxy (VCE)[7] which has been under development at Chevron for the past six years. This VCE technique combines many of the best properties of Molecular-Beam-Epitaxy (MBE) and Metal-Organic-Chemical-Vapor-Deposition (MOCVD) (see Figure 2)

to give higher materials utilization, easier scalability, improved safety, precise growth control, the convience of gas sources, and high quality semiconductor layers. A detailed description of VCE is given elsewhere.[8]

II. Single-Junction Device Performance

The theoretical efficiency limits of single-junction devices is being approached. Figure 3 shows the flash simulator I-V characteristics of GaAsSb and GaAs single-junction cells fabricated at Chevron. At these 99X and 59X AM0 concentration ratios, the active area efficiencies of both devices is 20.5%. Their measured external quantum yields peak at over 90% as shown in Figure 4. These indicate long diffusion lengths. In fact, an electron diffusion length of 10 microns has been measured in Chevron fabricated p-GaAs using a a curve fitting technique and a specially configured n^+-p sample.[9] This fitting result is shown in Figure 5. Such diffusion lengths exceed the device layer thicknesses by factors of from 3-10 and provide for near maximum current performance. Precise diffusion length measurements on actual high performance solar cells is not possible due to the inseparability of surface from bulk effects.[10] However, Figure 6 shows the theoretical fit of the 20.5% GaAsSb sample's internal quantum yield with a 7-micron value for electron diffusion length using Hovel's theoretical equations[11] and assuming the top surface recombination velocity is 10^4 cm/sec. Also, we assumed that the optical absorption edge is softened[9] and that the optical absorption coefficients are determined by Kuphal and Dinges' shift[12] of GaAs values to the 1.35 eV GaAsSb band gap.

The above 20.5% AM0 efficiencies illustrate the state-of-the-art performance now possible in III-V based solar cells. For comparison, Varian[13] recently reported a 21% AM0 efficiency GaAs solar cell. The practical performance limits of such standard single-junction devices has been estimated at 24% AM0 at NASA.[14] This is identical to the peak efficiency recently calculated by Chevron. For the latter estimate, see Figure 12 of Reference 15 (or Figure 19 of this report) and note that the single-junction performance is given by the zero-energy-band-gap-difference intercept. As this 24% limit is approached, comparatively large efforts will be required to achieve increasingly small improvements in performance.

III. Two-Junction Mechanical Stack Performance

A. Small Area GaAsP Cell

The highest performance $GaAs_{.7}P_{.3}$ devices fabricated at Chevron on GaP substrates have been of small area (0.0386 cm^2). The spectral response of the best such device is shown by the circular data points in Figure 7. The light I-V properties of this cell were measured in a xenon flash simulator and are plotted in Figure 8. The AM0 efficiency is 13.6% at the I_{sc} value of 19.5 mA that corresponds to a concentration ratio of 27X.

The device was formed on a lightly doped LED wafer fabricated by Hewlett-Packard with a layer graded in composition from GaP to $GaAs_{.35}P_{.65}$ over 10 microns followed by a 10-micron buffer layer of constant $GaAs_{.35}P_{.65}$ composition. At Chevron an additional transition was grown to a $GaAs_{.7}P_{.3}$ composition in two steps over 1 micron before the 3-micron thick p-n junction of $GaAs_{.7}P_{.3}$ was formed. More details of this device's fabrication by VCE are given elsewhere.[16] Because of the difficulty in making ohmic contact to the lightly doped GaP (mid-10^{16} cm^{-3}), both sets of contacts were made from the frontside of this small area device using interdigitation.

B. Large Area Si Cell

The spectral response of a large area (0.317 cm^2) Si cell is shown by the square data points in Figure 7. These data were obtained with the Si cell placed under a GaP wafer which was doped to n=2(10^{17}) cm^{-3} and coated on both sides with a two-layer antireflection coating (800 Å Ta_2O_5, 750 Å SiO_x) using an E-beam evaporator. The sharp cutoff of the short wavelength spectral response at 550 nm is due to the GaP absorption edge at 2.25 eV. An estimate of this Si cell's performance as the bottom cell in the stack is shown by the dashed line of Figure 7 that cuts off the short wavelength response at the 700-nm (1.8-eV) edge of the top cell. Convolving this truncated response with the AM0 spectra[17] specifies the short circuit current density of this device in the stack. The flash simulator measurement of this cell's light I-V properties are shown in Figure 9. From the calculated short circuit current density, this corresponds to an AM0 efficiency 7.11% at a 50X concentration ratio. This Si cell was made by M/A-COM, PHI, Inc., according to specifications provided by Sandia Laboratories for a mechanically stacked, bottom cell for concentrator applications.

An estimate of the combined efficiency of these cells in a stack is obtained by summing their individual performance values as shown in Table 1. The resulting total is 21% AM0. This exceeds the values achieved with monolithic, two junction cells and is of the same order as (but less than) the best efficiencies recently achieved in single-junction devices under concentrated light.[8,18,19]

Table 1

Measured AM0 efficiencies of a small area $GaAs_{.7}P_{.3}$/GaP top cell and a large area Si bottom cell for a mechanical stack.

	Eff. (%)	Conc. Ratio
$GaAs_{.7}P_{.3}$ on GaP	13.6	27*
Si Under GaAsP/GaP	7.1	50*
Sum	20.7%	

*These concentration ratios differ because the two devices were originally measured for a terrestrial AM1.5 sunlight spectra. Converting to space AM0 spectra changes the concentration ratio. Concentrator cell efficiency changes slowly with factor-of-2 changes in concentration ratio. This is shown in Figure 4 of Reference 19. It is also indicated in Figure 15 of this report for specific contact resistance values of 10^{-4} ohm-cm^2 and below.

C. Large Area GaAsP Cell

Recently the fabrication of large area $GaAs_{.7}P_{.3}$ cells on GaP has begun. Figure 10 shows a photograph of one of these along with a M/A-COM PHI, Inc. Si cell. The circular grid pattern is 0.25-inch diameter (0.317 cm^2 area), and it appears on both the top

and bottom of the GaAsP/GaP device. It is identical to the Sandia specified design for the Si cell. The grid consists of five concentric rings of 0.00937-, 0.0187-, 0.0374-, 0.0749-, and 0.125-inch radii filled, respectively, by 8, 16, 32, 64, and 128 radial grid fingers of 8-microns width that give 7% grid shading.

A special mask set was developed at Chevron to accommodate the special problems involved in stacked cell research and development. For example, the mask produced grid alignment marks can be seen as the two- and three-element, box-shaped patterns near the four corners of the GaAsP/GaP device in Figure 10. Since these edges are transparent GaP, these marks allowed the front and back grid patterns to be aligned to within 1 micron using a standard mask aligner. At the left side of the GaAsP/GaP device is an approximately 1/8-inch square diode with no grid lines. This region is used for measuring spectral response without the confusion of grid line reflectance and shading. It also provides sufficient unobstructed area for depth profile etching with the electrochemical profiler. At the bottom left of the GaAsP/GaP are four contact pads that are used to determine the contact resistance between the grid metalization and the top p-layer of the cell and the sheet resistance of the p-layer using the transmission line technique.[20] At the bottom right of the GaAsP/GaP is a small area diode used for log I-V characterization. All of these extra structures are for diagnostic purposes. They will be removed with a diamond wafering saw before the device is placed into a stacked package.

The dark and light I-V curve of one of these large area $GaAs_{.7}P_{.3}$ cells (Run 2) is shown in Figure 11. The open circuit voltage is 1.0 V and the fill factor is 0.7. The measured internal quantum yield spectra are shown in Figure 12 for the three, large-area-cell growth runs that have been completed so far. The successive runs are marked 1, 2, and 3, respectively, and the best efficiency achieved in these initial experiments is less than five percent. For reference, the fourth top curve of Figure 12 gives the best external quantum yield achieved with the small area cell formed on a LED wafer. The reasons for the successive improvements in Runs 1-3 and the remaining large area cell problems to be solved can be seen from the electrochemically etched depth profiles in Figure 13. The cell formed in Run 1 had a p-layer doping that was too high (10^{19} cm^{-3}) and a p-layer thickness that was too large (0.7 micron). This was corrected in Runs 2 and 3. We discovered a water leak in the system after all the growths were completed. This leak partially accounts for the difference between the best

large area device performance and that of the small area device on the LED wafer. The crucial importance of eliminating water vapor for high device performance has been detailed elsewhere.[9,21] The other remaining problems are the thickness and doping of the transition layers and the thickness of the n-layer. For these large area devices, a transition layer thickness of 3-4 microns was used with 14 individual step changes in P composition. (See Figure 13 for evidence of some of these transition layer steps.) According to the recent results of Wanlass et al.,[22] a transition layer of five or more microns is required. This is consistent with our best small area device formed on a LED wafer, which had a 10-micron thick transition region. Furthermore, a typical n-layer thickness for a high-efficiency Chevron cell has been on the order of 3-4 microns. The constant composition n-layer for the high-quantum-efficiency, small area cell on the LED wafer was 10 microns. However, these first GaAsP/GaP, large area experiments used a constant composition n-layer thickness of less than 2 microns. (See Figure 13.) This n-layer dimension needs to be explored with further experiments. Finally, the electrochemical profiles show that all growths have a high resistance region in the transition layer that is doped with less that 10^{16} cm^{-3} carriers. This can be corrected by performing flow rate calibration runs for doping the highest P-content portions of the transition layers.

The above illustrates the methodical characterization used to assess the devices under development and the way that appropriate experiments are defined to solve each problem as it is identified. These also show the stage of the development as of the end of the present Air Force contract and indicate the next work required to produce high performance, large area, stackable, GaAsP/GaP solar cells.

This first growth of the large area GaAsP/GaP cells described above involved the simultaneous solution to seven challanging problems. These are: (1) the heat transfer problem for the growth of GaAsP onto free-standing GaP wafers using free moly blocks, (2) the incorporation of large fractions of P using the thermal cracker, (3) the reduction of free carrier absorption using low doped GaP substrates, (4) the reduction of the contact resistance to the GaP using a multilayer metalization and anneal, (5) the design and production of grid masks using a computer optimization program, (6) the alignment of the front and back surface grid patterns using alignment marks at the transparent edges of the GaP substrates, and (7) the processing of the semiconductor wafer without damage using a series of protective layers. The grid alignment was described

above and the other six problems are discussed in the paragraph and sections below.

The free-standing GaP wafers were required to allow processing both the top and bottom surfaces of the GaAsP/GaP device. Ample thermal coupling of the GaP to the radiant heater was obtained by setting moly blocks on top of the GaP wafers without any bonding. (See Figure 2.) Since no bonding agents were used, the GaP surface was left undamaged for later processing. Large amounts of P incorporation were required to allow transition layer growth with $GaAs_{1-x}P_x$ compositions all the way up to GaP. Preheating the PH_3 to 800°C before it entered the 700°C reaction chamber (see Figure 2), allowed any desired compostion to be formed. Without the thermal cracker, layers could only be grown in the VCE reactor with 50% or less of the As replaced by P in the GaAsP. For the small area device on the LED wafer, the P incorporation problem was circumvented by purchasing the GaP substrate from Hewlett-Packard with a 10-micron wide transition already grown down to a $GaAs_{.35}P_{.65}$ composition. Hewlett-Packard used one atmosphere halide transport CVD for this growth. For the 300-micron GaP substrates of the current work, there was excessive absorption of sub-band-gap photons by free carriers until the doping was reduced to $2\ (10^{17})\ cm^{-3}$. The processing of both top and bottom surface grid patterns required special processing techniques. Table 2 gives the outline of the two sided processing with protective coatings of Lacomit[23] applied at appropriate times to the various surfaces (see Steps 1-1,3-3, and 5-2 from Table 2) to protect against chemical and physical damage during cell fabrication. Each procedure of Table 2 involved 4 to 20 steps. More than 220 individual processing steps were used for each large area GaAsP/GaP device.

Table 2

Large Area Cell Processing Procedures
(After Epitaxial Layer Growth)

Outline

1-0 Metalized Backside of GaP Wafer

- 1-1 Degrease Wafer and Apply Lacomit to Frontside
- 1-2 Etch Reaction Residue and Oxides Off Backside
- 1-3 Apply Grid Photoresist Pattern to Backside
- 1-4 Toluene Harden Photoresist and Develop
- 1-5 Deposit AuGe/Ni/Au Back Metalization and Lift Off
- 1-6 Anneal Grid Metalization

2.0 Isolate Front Bussbar

- 2-1 Apply Isolation Photoresist Pattern to Frontside
- 2-2 Deposit Ta_2O_5 Layer
- 2-3 Deposit Ti/Ni/Au Coatings on Ta_2O_5 Layer and Lift Off

3-0 Metalize Frontside of Wafer and Final Anneal

- 3-1 Apply Grid Photoresist Pattern
- 3-2 Toluene Harden Photoresist and Develop
- 3-3 Protect Backside with Lacomit
- 3-4 Etch Through Window Layer
- 3-5 Deposit Ag-Mn Front Metalization and Lift Off
- 3-6 Anneal Sample

4-0 Plate Grid Patterns

- 4-1 Apply Grid Photoresist Pattern to Frontside
- 4-2 Silver Plate Front Grid (Oxidation Concern Terminated)
- 4-3 Apply Grid Photoresist Patern to Backside
- 4-4 Silver Plate Backgrid

5-0 Isolate Device

- 5-1 Apply Mesa Photoresist Pattern to Frontside
- 5-2 Apply Lacomit to Backside
- 5-3 Hard Bake After Developing
- 5-4 Perform Mesa Etch

6-0 Measure, Antireflection Coat, and Test Device

- 6-1 Measure Spectral Response and Light I-V
- 6-2 Measure Electrochemical Profile
- 6-3 Apply Ta_2O_5 and SiO_x (A.R.) Layers
- 6-4 Measure Spectral Response and Flash I-V

IV. Other Properties of GaAsP on GaP and of a Mechanical Stack

A. Edge Heat Removal

One advantage of a thick GaP substrate is that it allows a major fraction of the heat load in the top device to be conducted through the GaP substrate edges. Thus all of this heat does not have to pass through the bottom device. A mounting fixture that exploits this edge heat dissipation is shown in Figure 14. The top heat spreader conducts the edge heat out through the spacers at the edge of the package. This relaxes the requirements on any adhesive used to bond the top and bottom cells together.

For example, a 20°C temperature rise would be enough to conduct 2/3 of a 400X top cell heat load (7 watts/cm^2) to the edges of a 250-micron thick GaP wafer (77 watts/m-C thermal conductivity) with a 1/4-inch diameter solar cell. The remaining 1/3 of the heat can be conducted to the bottom cell through a RTV-615 adhesive film (0.19 watts/m-C thermal conductivity) of 7.5 microns thickness. This 7.5 microns is wide enough to absorb the thermal expansion mismatch stresses without fracturing.[24] If all this heat had to pass through the adhesive with no more than a 20°C temperature rise, the adhesive may have to be too thin to absorb the expansion mismatch or to provide adequate voltage isolation. With a 20-V/micron dielectric strength, the 7.5 microns of RTV-615 would provide a 150-V stand off between the top and bottom cells.

The above temperature drop and heat flow calculations were estimated with the following expressions. The temperature rise consists of two components T^O and T^1. The first is given by[25]

$$T^O = \frac{Q}{4\pi tK} \tag{1}$$

where T^O is temperature drop from the center of the circular GaAsP/GaP cell out to its 0.25-inch diameter circumference, t is the 250-micron thickness of the GaP substrate of thermal conductivity K (K = 46 and 77 W/m-°C for GaAs and GaP, respectively), and Q is the total heat load (watts). The second component T^1 accounts for the estimated 2-mm spacing from the above 0.25-inch diameter circumference to the surrounding heat sink. This is given by[25]

$$T^1 = \frac{Q}{2\pi tK} \ln (R_1/R_0) \tag{2}$$

where R_0 is half the 1/4-inch cell diameter and R_1 equals R_0 plus the 2-mm spacing to the heat sink. The above are conservative, over estimates of the temperature rise in that the heat conduction of the metal grid fingers was neglected.

B. Effect of Contact Resistance to n-GaP

The calculated concentration ratio dependence of the efficiency of the $GaAs_{.7}P_{.3}$/GaP top cell is shown in Figure 15 for the Sandia grid pattern. For the case of zero contact resistance losses (R_c=0), the design is optimized for 120X AM0 (or 200X AM1.5D) concentration; and it gives less than one-half absolute percent loss in efficiency out to 500X AM0 (or 800X AM1.5D). This was calculated with the Basore expressions[26] for grid shading loss and resistive losses in the semiconductor layers and the grid metalization.[27] The additional effects of contact resistance losses were obtained with the expression of Cape et al.[28] As shown, the contact resistance losses become substantial as R_c increases from 10^{-4} to 10^{-3} ohm-cm^2. At 10^{-5} ohm-cm^2, the R_c losses are negligible. The contact resistance of the backside grid to the n-GaP wafer (with n=$2x10^{17}$ cm^{-3}) was reduced to the 10^{-4} ohm-cm^2 by the use of a multilayer metalization (400 Å 88%Au-12%Ge(wt)/300 Å Ni/400 Å Au), applied in an E-beam evaporator and annealed in forming gas at 450°C for 60 sec. This is a factor of 4 less than the lowest values reported in the literature[29] for n-GaP doped into the low 10^{17} cm^{-3} range, and it is crucial for adequate cell performance at concentration as indicated by Figure 15. The $2(10^{17})$ cm^{-3} GaP doping is required because of the substantial absorption losses measured at Chevron with n=$8(10^{17})$ cm^{-3}. This is due to free carrier absorbtion.[30] The low R_c values are difficult to measure.[20] The 10^{-4} value was obtained with the Cox and Strack method[31] of curve fitting measured resistances as a function of circular contact diameters, using contact diameters down to 40 microns. This R_c curve fit analysis is shown in Figure 16.

C. Effect of GaP Spreading Resistance

Hall measurements of a typical GaP substrate gave an electron concentration of $2.6(10^{17})$ cm^{-3} with a mobility of 110 cm^2/V-sec. and a resistivity of 0.22 ohm-cm. This resistivity value agrees with the similar resistivity obtained from the Cox and Stract analysis as shown in Figure 16. It determines the spreading resistance contributions to series resistance losses due to the backside grid. This loss was not included in the Basore analysis[26] of Figure 15. The geometry involved is illustrated in Figure 17A with the 8-micron wide grid fingers, 134-micron average grid spacing,

and 300-micron GaP thickness. This resistance is a microstrip transmission line geometry that has not been solved analytically.[32] However, bounds can be set using the exact solution for the coaxial resistor shown in Figure 17B. Here, r_1 is equal to half the grid finger width.

For a grid line of length l, the total resistance R_T of a Figure 17B coaxial resistor due to the specific contact resistance R_c and due to the bulk resistivity ρ of the material (i.e., the spreading resistance R_s), is given by

$$R_T = \frac{R_c}{2r_1 l} + \frac{\rho}{\pi l} \ln(r_2/r_1) \tag{3}$$

so that the ratio of spreading-resistance-to-contact-resistance contribution to series resistance R_s^*/R_c^* is given by

$$\frac{R_s^*}{R_c^*} = \frac{2\rho\, r_1 \ln(r_2/r_1)}{\pi R_c} \tag{4}$$

where the asterisk superscripts indicate that the actual values of the series resistance contributions will vary depending on the total length of the grid lines and the relative magnitude of the current along the grid lines. However, this ratio remains constant independent of this length or the current variation.

Approximate lower and upper bounds are determined by letting r_2 equal half the grid spacing (67 microns) and the 300-micron GaP thickness, respectively. The resulting ratio of spreading-to-contact contribution to series resistance R_s^*/R_c^* is shown in Figure 17C as a function of the specific contact resistance R_c. For the R_c of 10^{-4} ohm-cm^2, the spreading resistance loss is 2.5 to 3.5 times larger than that of R_c. The resulting loss in efficiency is approximated by the $3(10^{-4})$ ohm-cm^2 curve of Figure 15.

Note that the r_1/r_2 ratio is the shading fraction of the grid pattern when r_2 equals half the grid spacing (and $r_2 >> r_1$). Thus the spreading resistance R_s (estimated by the second term of Equation 3) is largely determined by this grid shading (and by ρ) independent of the exact grid finger width dimension itself.

The spreading resistance loss of the front grid was included in the Basore calculation.[26] Its effect is much smaller than that of the back grid due to the factor of five lower resistivity of the

top p-GaAsP layer which has a five times higher doping level and a majority carrier mobility similar to that of the n-GaP wafer. The back grid spreading resistance limitation can be alleviated by doping the 0.5 to 1 micron GaP layer next to the bottom grid to the 10^{18} cm^{-3} level. This is thin enough to not reduce the GaP transparency significantly by free carrier absorption but is still thick enough to strongly reduce the spreading resistance.

D. Four-Terminal Voltage Matching

The four-terminal property of a mechanical stack (Figure 14) allows more versatility in interconnecting the junctions than does a monolithic stack. In particular, it allows voltage matching of the cells. Figure 18 illustrates the 2 x 4 wiring scheme that can be used to voltage match four terminal cells whose upper and lower devices differ in output voltage by a factor of 2. From Figures 8 and 9, the voltage ratio of our GaAsP and Si cells is about 1.62 which can be closely matched by a 13 x 8 generalization of the Figure 18 wiring scheme. Of course the GaAsP composition can also be adjusted to change this voltage ratio to 2:1. Output voltages vary only logarithmically with current. Thus voltage matching has definite advantages in applications where current changes are anticipated. This would be found in space where the radiation damage decay rate in current would be different in the GaAsP and the Si junctions.

V. Projected Efficiency Calculations

A. Projected AM1.5D Efficiency of $GaAs_{.7}P_{.3}$ in a Two-Junction Mechanical Stack

The potential performance capability of $GaAs_{.7}P_{.3}$ junctions has been assessed with the theoretical expressions of Hovel.[11] An efficiency of 19.5% for 100X of AM1.5 direct normal (AM1.5D) light[33] is obtained for 4-micron diffusion lengths, 0.5-micron junction depth, good surface passivation, and optical absorbtion coefficients specified by shifting GaAs values to a 1.8 eV band edge using the procedure of Kuphal and Dinges.[12] Combined with the Si efficiency of Figure 9, a mechanical stack efficiency of 28% AM1.5 is predicted for this materials combination. For an optimized Si cell this combined efficiency could rise to 29% AM1.5D. Achievement of these performance levels awaits the full development of the $GaAs_{.7}P_{.3}$ junction with sufficient materials quality and surface passivation and with appropriate transition layers to the

GaP substrates of proper quality for long diffusion lengths and low surface recombination.

Silicon cells have the advantage of being a fully developed and readily available technology that performs at near their theoretical limits. They have the disadvantage of being an indirect transition material with a soft absorption edge, that causes a falling spectral response at long wavelengths shown in Figure 7. A direct gap material, like GaInAs or GaAsSb, has a sharper absorption edge at the 1.1 eV (1100 nm) band edge as has been verified by Lewis et al.,[34] and Gee.[35] This provides for increased current output in a two-junction stack. The projected efficiency of such a bottom device under a 1.8 eV top cell is 13.7% AM1.5D at 100X for the same assumptions as the preceding paragraph. This raises the potential combined AM1.5D efficiency to 33.2%. So far efforts to improve the long wavelength response of Si cells have given higher Si currents but not higher efficiency in a stack.[35]

B. Projected AM1.5D Efficiencies of Other Two-Junction Mechanical Stacks

The two-junction stack efficiencies have been calculated for numerous band gap combinations and are plotted in Figure 19 as a function of the band gap difference. The assumptions and theory of the first paragraph of this section were used. This clearly illustrates, for the first time, that it is the band gap difference that is one of the strongest determinants of two-junction efficiency. The efficiency of the top cell of each stack is given by the zero energy gap difference intercept. The efficiency of the bottom junction is found by subtracting this from the sum. With top-junction band gaps E_G(Top) ranging from 1.5 to 2.0 eV, all the efficiencies peak between 31.8 and 34.6% AM1.5 for a band gap difference of about 0.6 eV to 0.8 eV. The efficiency contribution of the top junction at the peak increases from 1/2 at 2.0 ev to 3/4 at 1.5 eV indicating the dominant role of the top device. This indicates the advantage of being able to use a very efficient top cell and allows the evaluation of alternate materials systems.

The starting point for the Figure 19 results was the open circuit voltage of 1.1 V and the fill factor of 0.82 that Chevron has measured on a high performance GaAs device.[9] Hovel's expressions (Reference 11, p 51-61) were then used to calculate changes in these two parameters with band gap. For the open circuit current voltage this involved the assumption of unity diode quality factor (A_O = 1) and noting that the preexponential term I_{OO} is

proportional to n_i^2 which is, in turn, proportional to $\exp(-E_G/KT)$ as given by Sze,[36] where E_G is the band gap. The result is that the open circuit voltages change is exactly the same as the band gap change. The change in fill factor (FF) with open circuit voltage was obtained from Hovel's Figure 34. The short-circuit current came directly from Hovel's equations for spectral response (Reference 11, p 18, 19, 25, and 37) assuming zero reflectance loss and the ASTM (AM1.5D)[37] values for the spectral distribution of the incident sunlight. The accuracy of Hovel's expressions for spectral response modeling is supported by the close fits to measured data such as shown in Figure 6. The results of these calculations for the performance of the top cell of the stack are shown in Figure 20. Here the open circuit voltage, short circuit current density, and the fill factor are given in addition to the top junction efficiency as a function of the top junction band gap E_G(Top). Similarly, the bottom junction's calculated efficiency and short circuit current densities are shown in Figures 21 and 22 as a function of the bottom cell's band gap for each top junction band gap value E_G(Top). The corresponding open circuit voltage and fill factors of the bottom junction are given in Figure 23. The minima and inflection points at 1.3eV band gap values in Figures 21 and 22 are caused by the sharp water vapor absorption line centered at 950 nm.[37] Such water vapor absorption is absent in the space environment. Note that the measured starting point values of GaAs for open circuit voltage and fill factor that were used in the calculations are less than the theoretical maxima given by Hovel. Thus the calculations given here are practically realizable values indicative of the best present performance levels achieved in GaAs. This makes these calculated values lower than the more idealized efficiencies such as given by Bennett and Olsen.[1]

An independent check of some of these predicted values can be obtained by comparison to experimental data. Recently, Sinton et al.[38] have fabricated point contact Si cells whose performance approaches the theoretical maximum possible with a 1.1 eV band gap converter. Their 25% AM1.5 efficient cells had open circuit voltages between 0.798 and 0.808 V and fill factors between 0.84 and 0.85 for light concentration ratios on the order of 80 to 150X. These compare to the 100X calculated 0.8 V open circuit voltage and 0.77 fill factor of Figure 23 for a 1.1 eV band gap. This indicates good agreement, but the calculated fill factors are low. The calculated fill factor of 0.805 and open circuit voltage of 1.05 V shown in Figure 23 for a band GaP of 1.35 eV compares to the recently reported[8] experimental fill factor of 0.85 and 1.07 V open circuit voltage obtained in a 1.35 eV GaAsSb junction of 26% AM1.5

efficiency with a 130X concentrated light ratio. Again, the voltages agree and the calculated fill factor is low. These are further indications that the Figure 19 efficiency projections are conservative.

C. Projected AM1.5D Efficiency of GaAs in a Two-Junction Mechanical Stack

A promising alternative mechanical stack, suggested by the above analysis, is to use a GaAs top cell. Recently, GaAs has achieved 26% AM1.5 efficiencies at concentration.[19] A GaAs 1.4 eV top band gap curve has not been calculated for Figure 19, but such a curve should be similar to the 1.5 eV band gap result. If the 26% AM1.5 performance can be maintained when this cell is grown on a thick GaAs substrate of low doping at $2(10^{17})$ cm^{-3} to avoid free carrier absorbtion[30] and with open-back grid for mechanical stacking, Figure 19 shows that a total combined AM1.5D efficiency of 30 to 31% should be achievable with a direct band gap bottom cell at 1.1 eV such as GaInAs or GaAsSb. Conventional Si cells (like Figure 9, not point contact configurations) have the same 1.1 eV band gap, but their soft response edge (Figure 7) could lower the bottom cell contribution by as much as 50% to a total stack efficiency of around 29% AM1.5D. The highest GaAs/Si stack efficiency reported so far is 25% AM1.5.[5] The 34% peak AM1.5D efficiency projected in Figure 19 occurs at around a 0.7 eV band gap difference between the two junctions using a direct material like GaSb for the bottom cell. With an indirect gap at 0.7 eV, a Ge bottom cell could provide for a stack total of around 31% AM1.5D. Other advantages of the GaAs top cell is that no lattice transition layers are needed to its substrate, no junctions are grown in the more complicated ternary materials, and spreading resistance limitations should be avoided due to GaAs's higher electron mobility.

D. Conversion From AM1.5 to AM0 Efficiency

The above projections were calculated for AM1.5 spectra. A first order estimate of corresponding AM0 values can be obtained by noting that AM0 efficiencies are approximately 0.9 times the AM1.5 values for two-junction stacks. This factor is indicated in References 15 and 16, and it was used to estimate the AM0 efficiencies at the right side of Figure 19. The resulting projections of AM0 efficiencies are greater than 27% for $GaAs_{.7}P_{.3}$/GaP stacked on 1.1 eV band gap GaAsSb or GaInAs or for GaAs stacked on Ge or GaSb.

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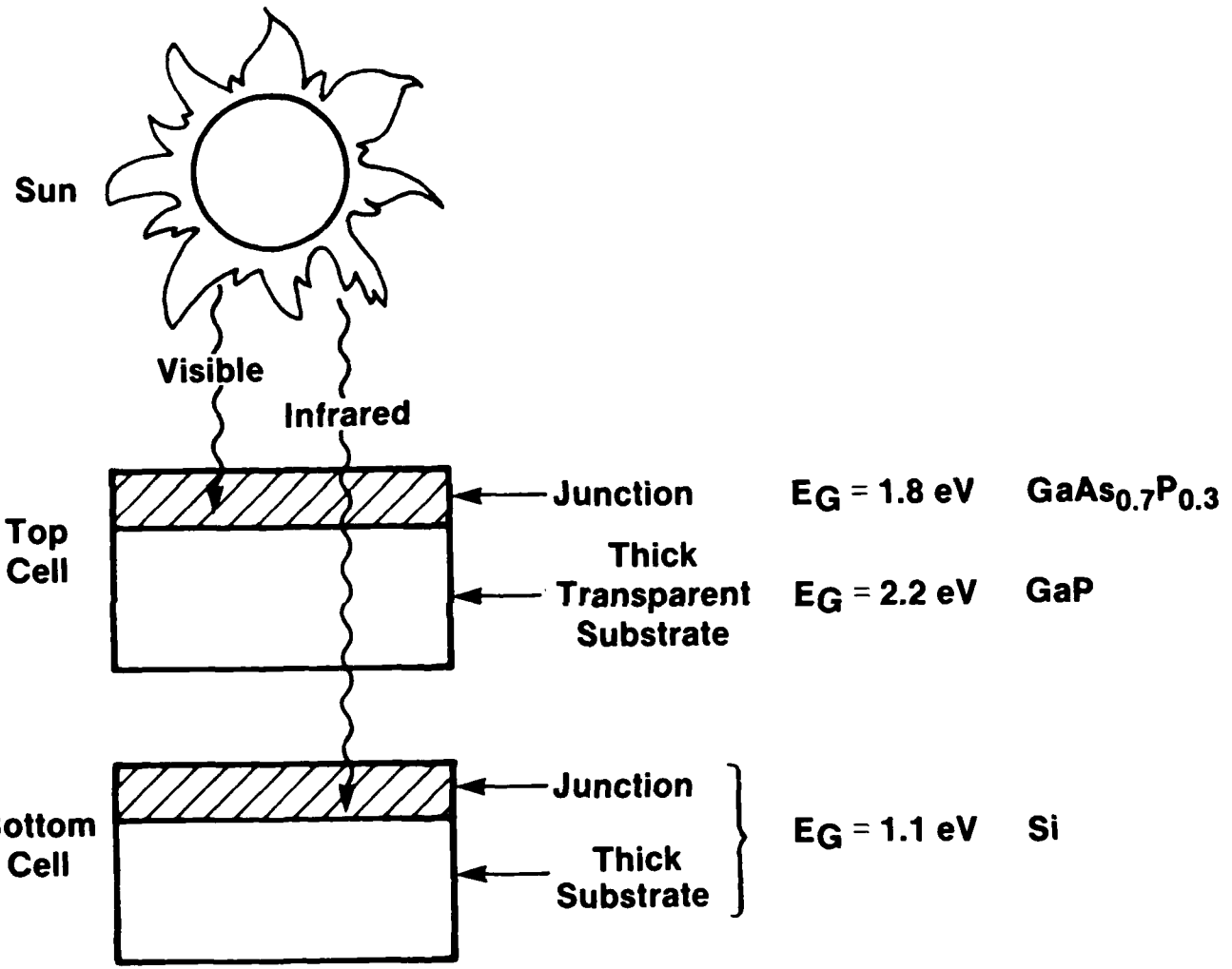


Figure 1 - Configuration for mechanically stacking a $GaAs_{0.7}P_{0.3}$ junction, formed on a thick transparent GaP substrate, unto a Si cell.

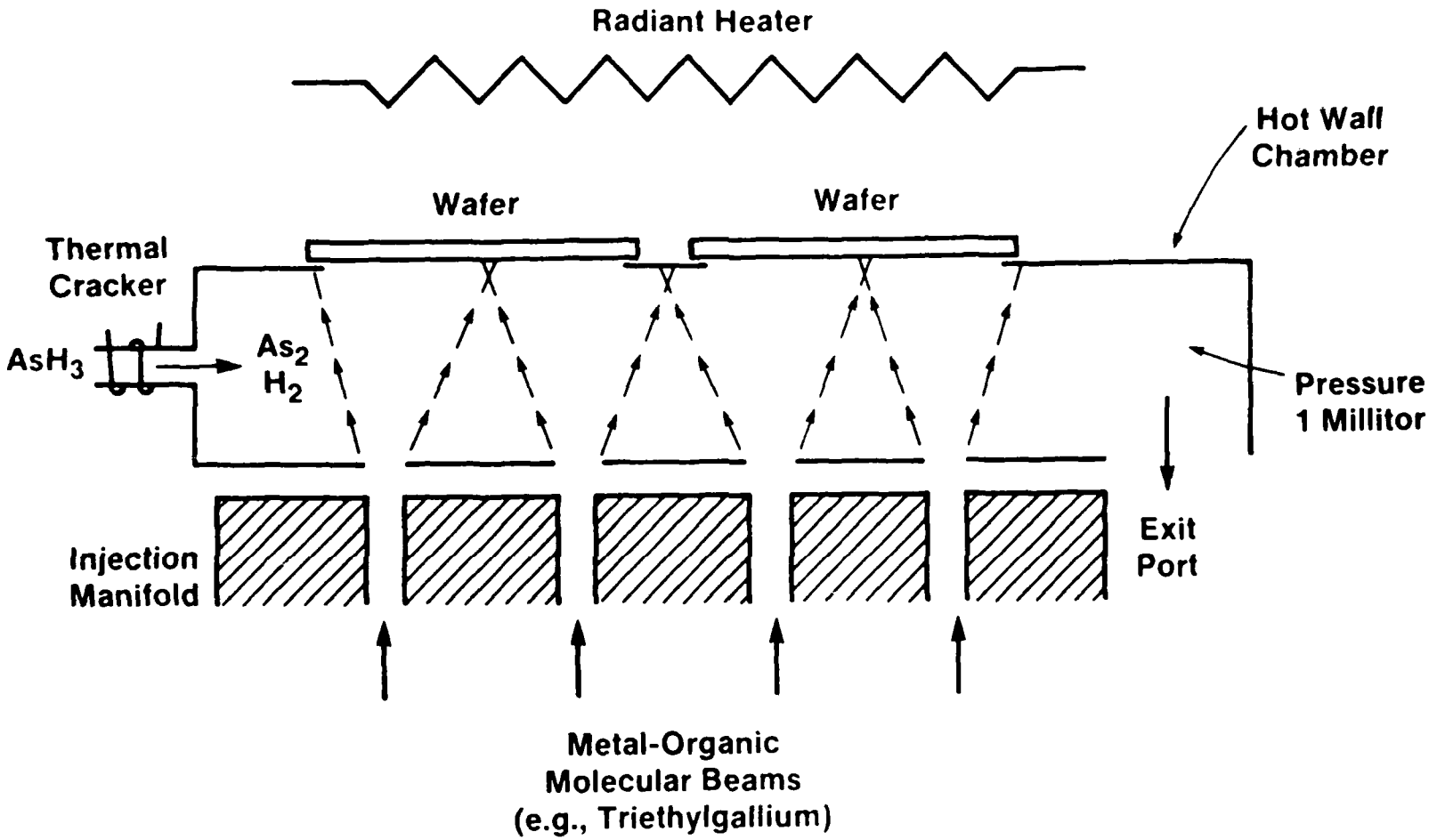


Figure 2 - Schematic diagram of the VCE process that combines the safety and control of MBE with the gas source convenience of MOCVD and provides for uniform depositions over large areas.

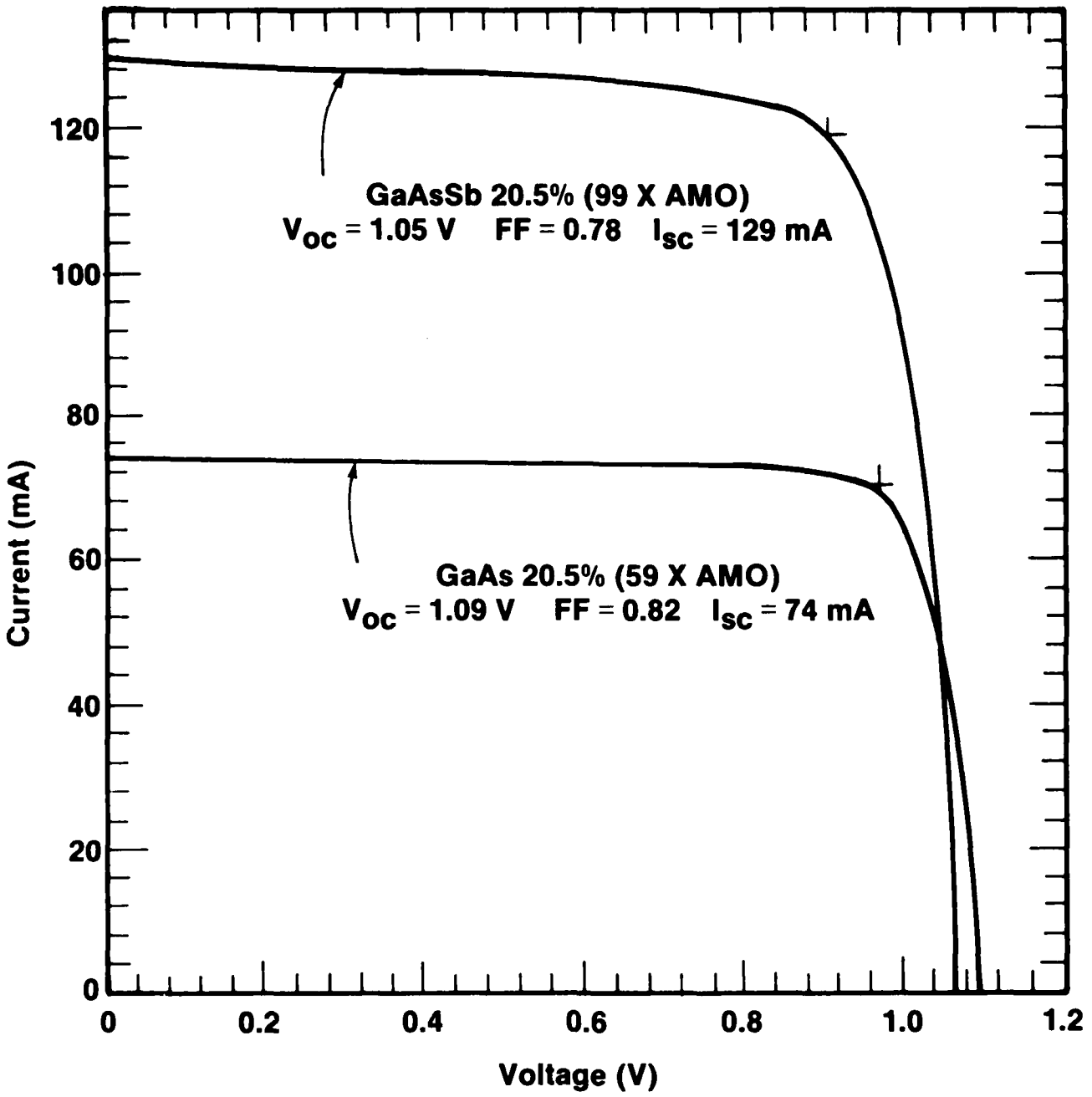


Figure 3 - The I-V characteristics of single-junction GaAsSb and GaAs solar cells measured in a xenon flash simulator.

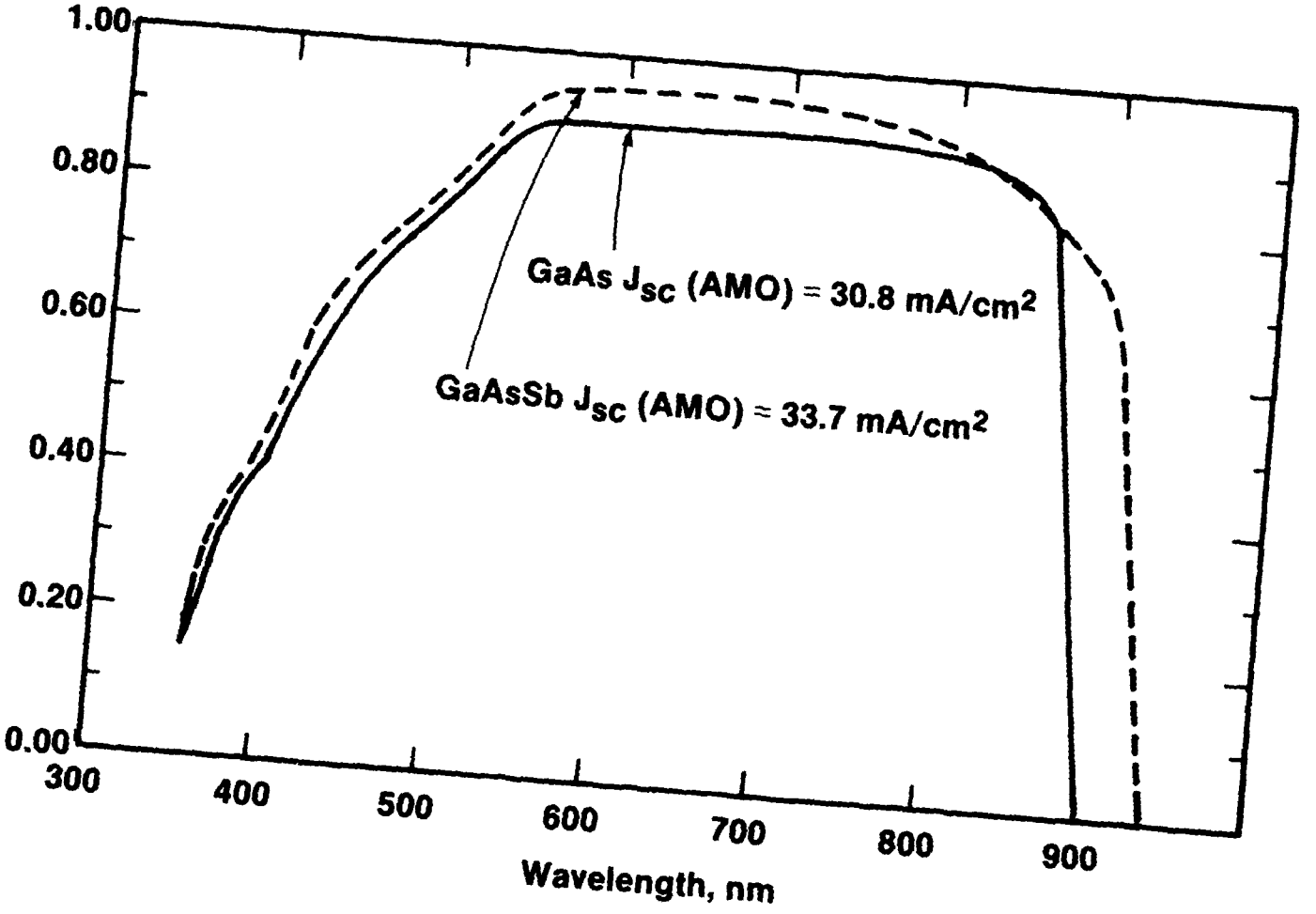


Figure 4 - The external quantum yield spectra measured on the GaAsSb and GaAs cells of Figure 3.

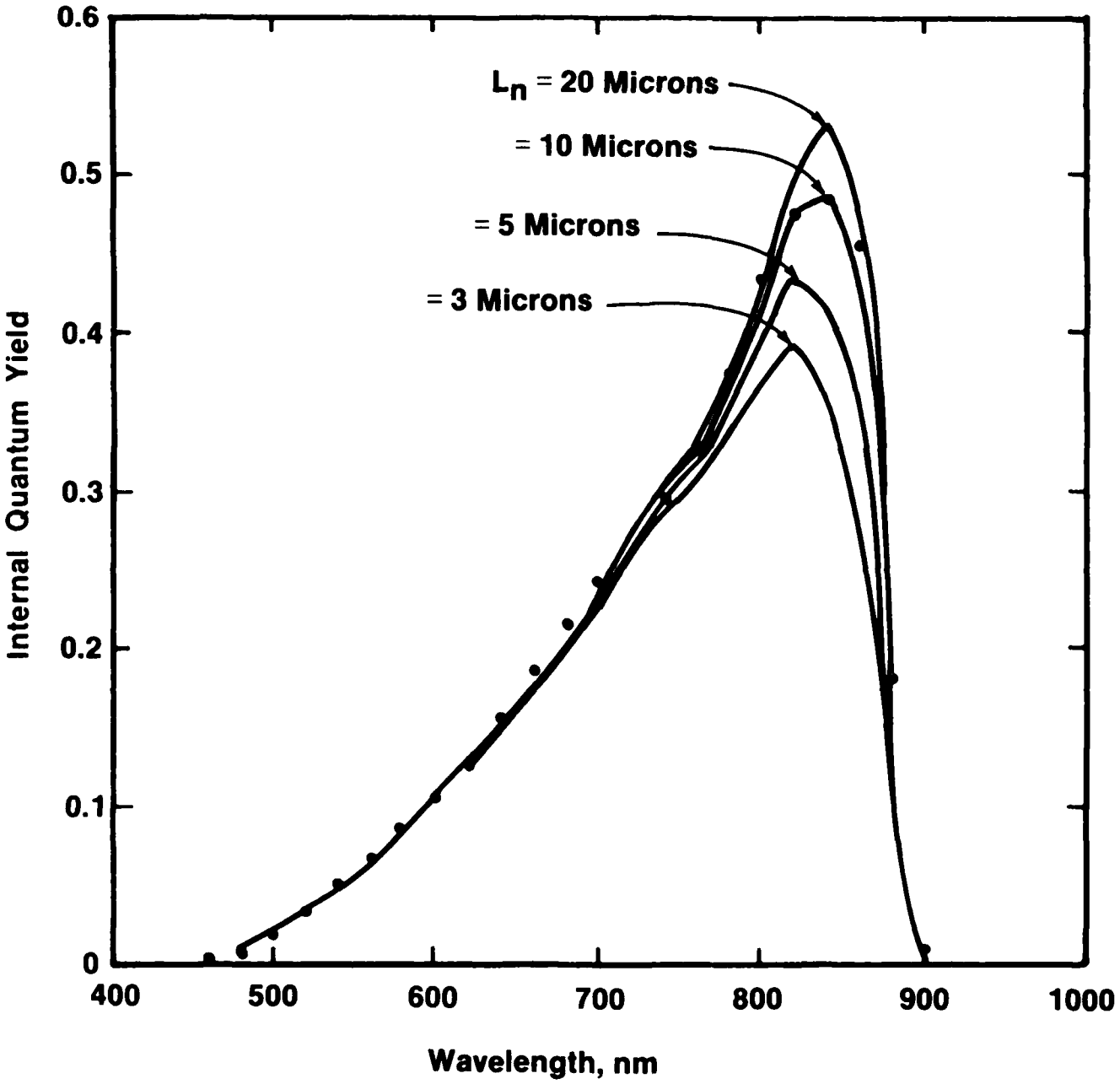


Figure 5 - A plot of the quantum yield spectra, curve fitting process used to measure a 10-micron electron diffusion length in p-GaAs using a specially configured n^+-p sample.

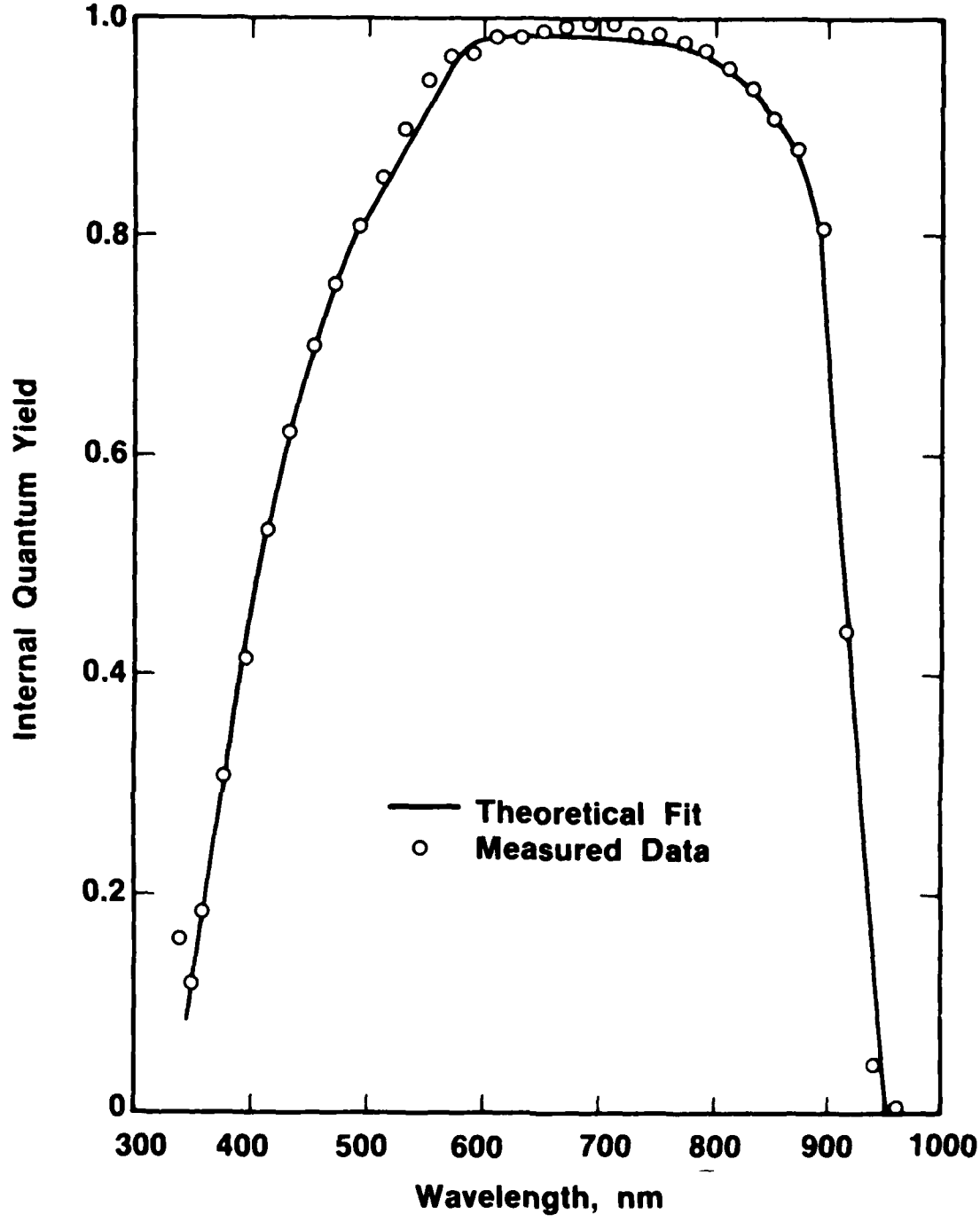


Figure 6 - THE FIT OF THE INTERNAL QUANTUM YIELD OF THE FIGURE 3 AND 4 GaAsSb CELL USING A SEVEN-MICRON VALUE FOR THE ELECTRON DIFFUSION LENGTH AND A 10^4 cm/SEC. SURFACE RECOMBINATION VELOCITY

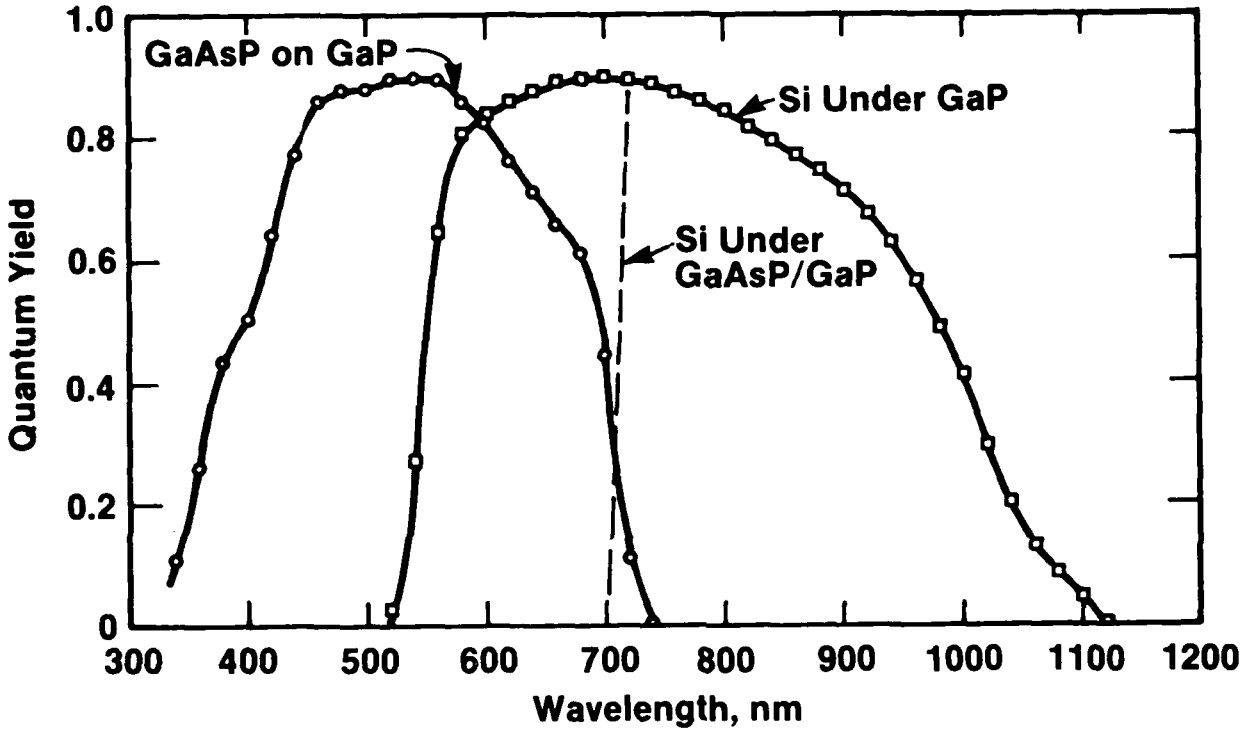


Figure 7 - The quantum yield spectra measured on the GaAsP junction grown on a GaP wafer and measured on the silicon cell under a GaP wafer. The broken line estimates how the Si response is truncated by a GaAsP cell.

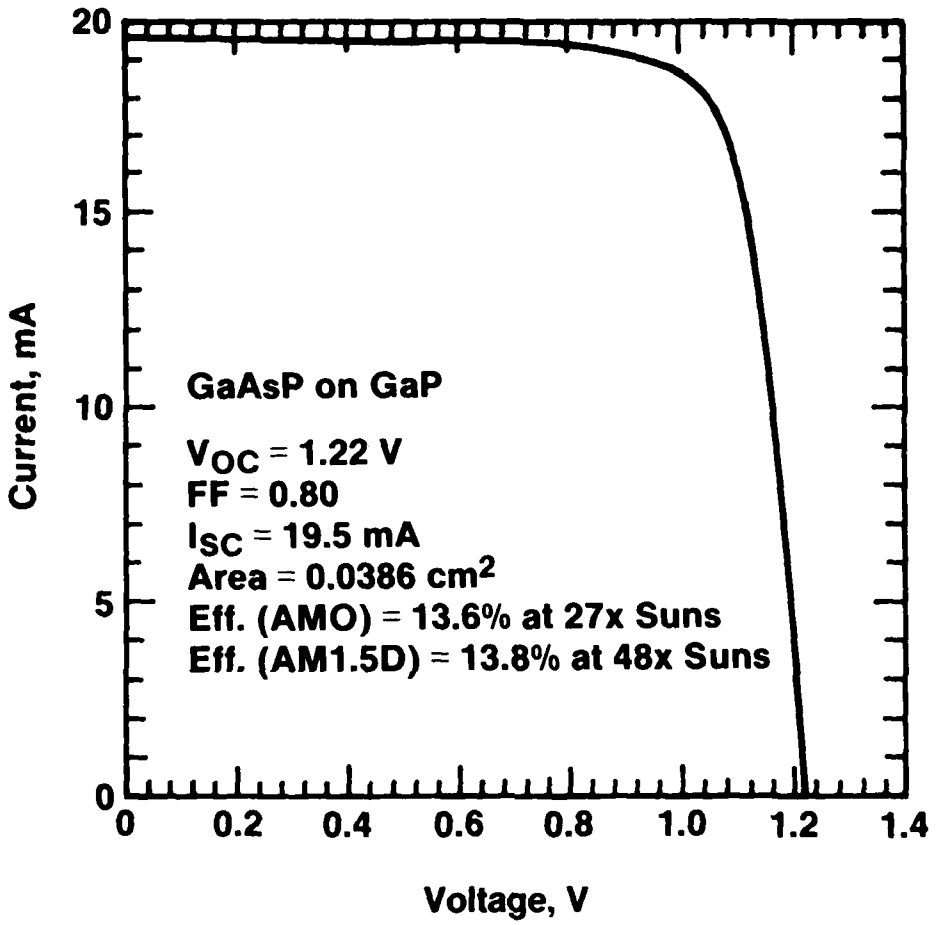


Figure 8 - The light I-V properties of a GaAsP on GaP cell measured in a xenon flash simulator.

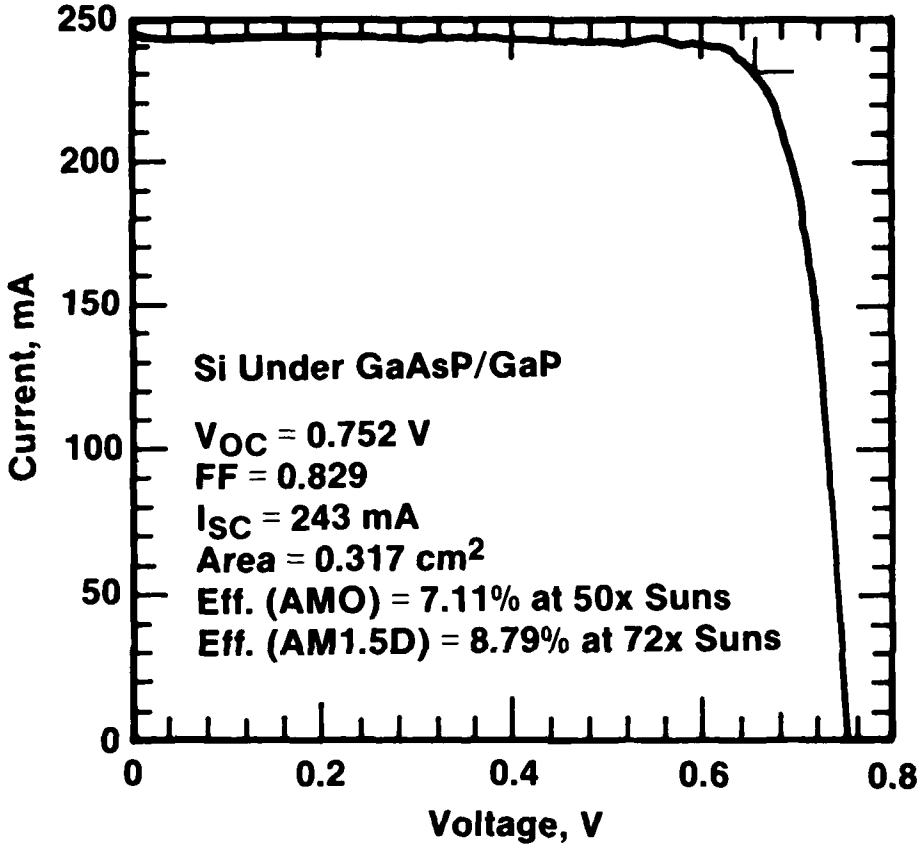
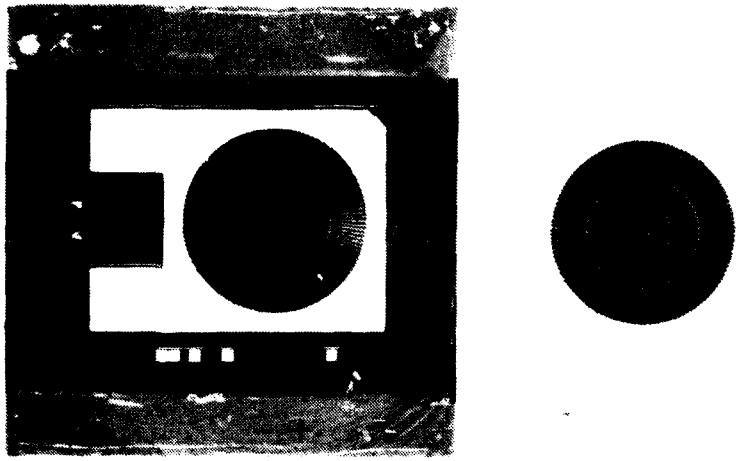


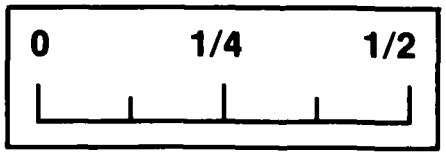
Figure 9 - The light I-V properties of a Si cell under the GaAsP/GaP device, measured in a xenon flash simulator.

Figure 10 - Photograph of the large area GaAsP on GaP and the large area Si cells configured for stacking with identical grid patterns.



$GaAs_{.7}P_{.3}$ on GaP

Si



Inch

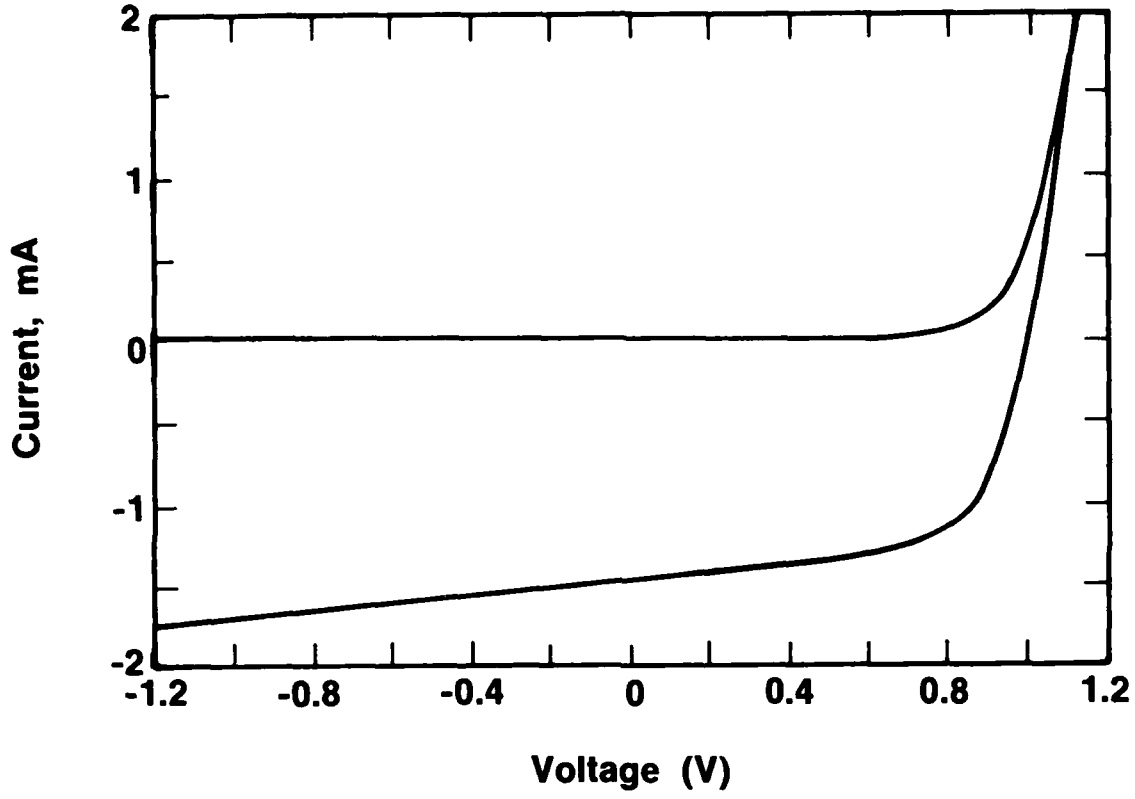


Figure 11 - The dark and light I-V characteristics of a large area $GaAs_{0.7}P_{0.3}$ junction formed on a thick, transparent GaP wafer.

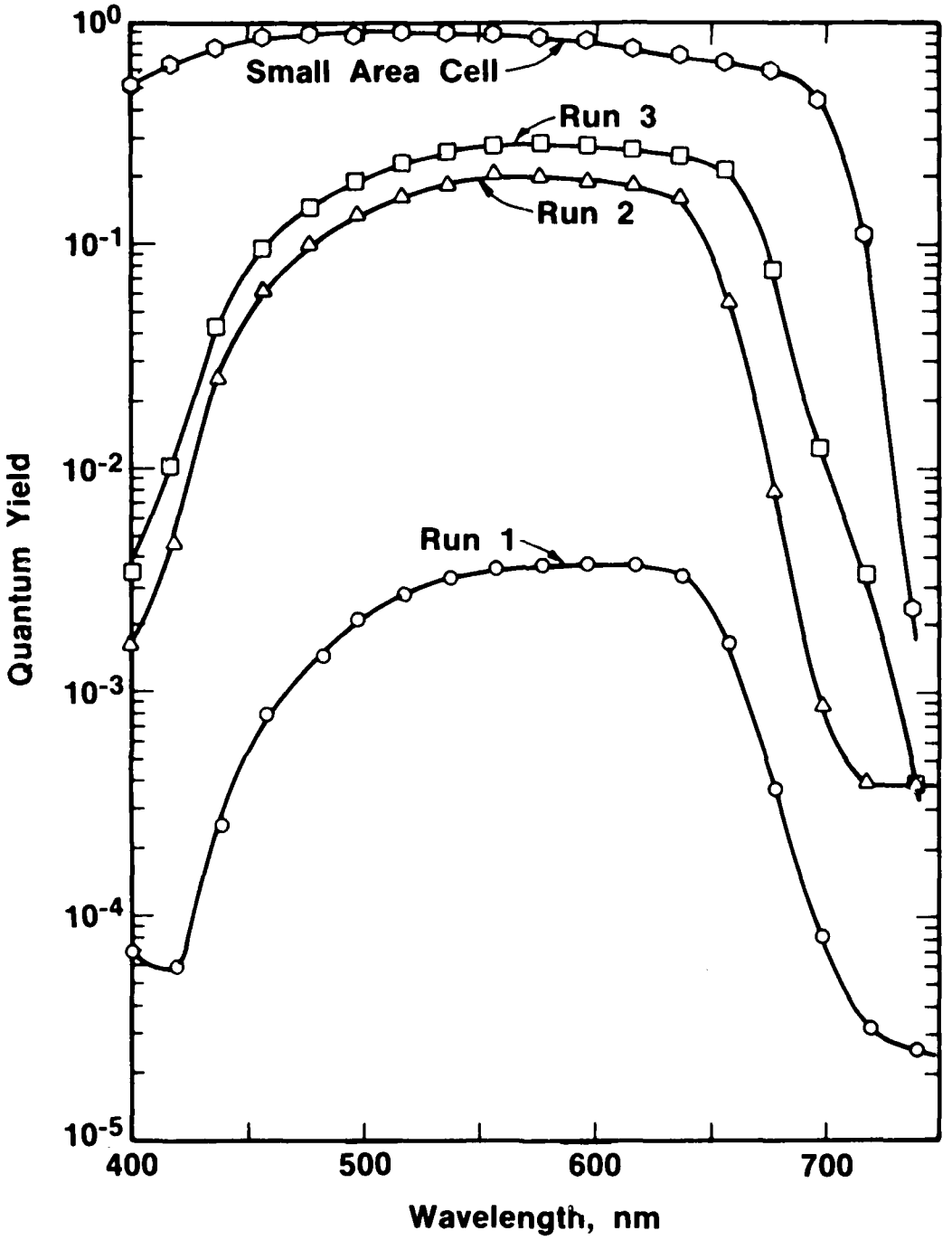


Figure 12 - The internal quantum yield spectra measured on large area GaAsP/GaP cells from Runs 1, 2, and 3 and the external quantum yield measured on the small area cell formed on the LED wafer.

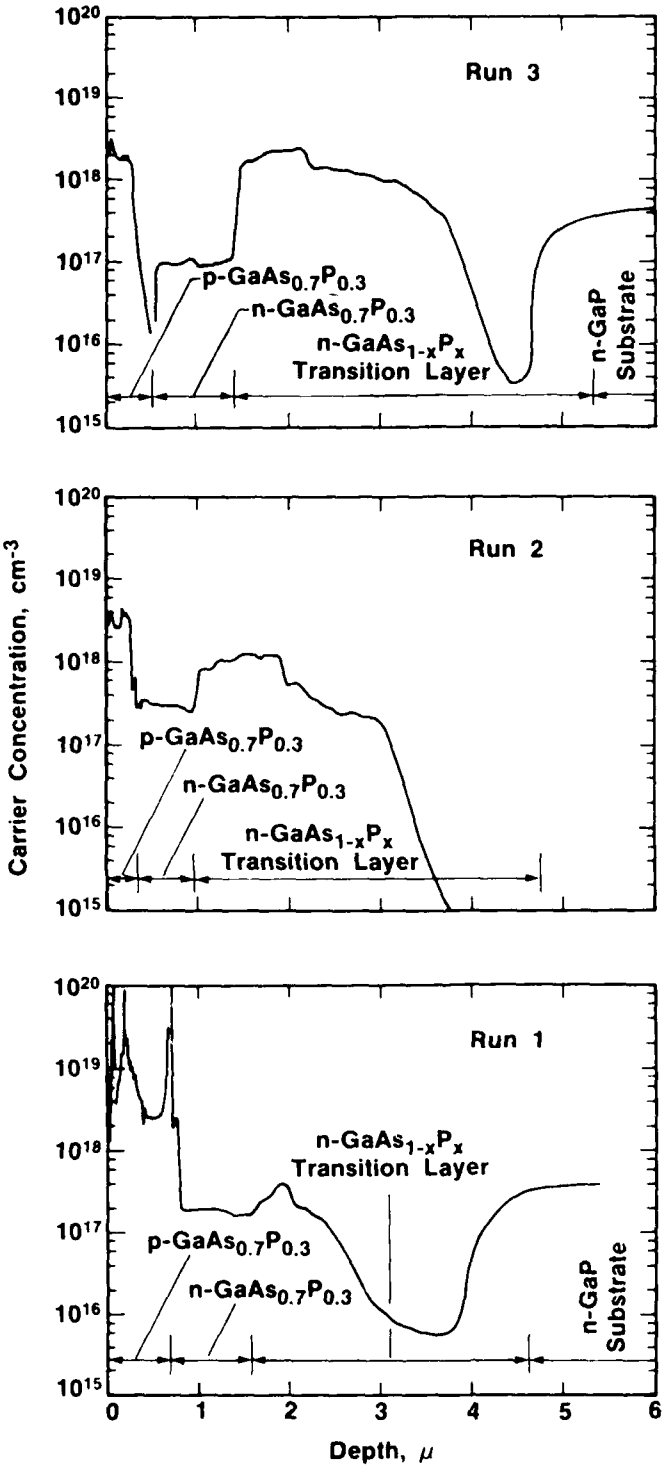


Figure 13 - The electrochemical profiler determination of carrier concentration versus depth for the three large area samples of Figure 12 from Runs 1, 2, and 3.

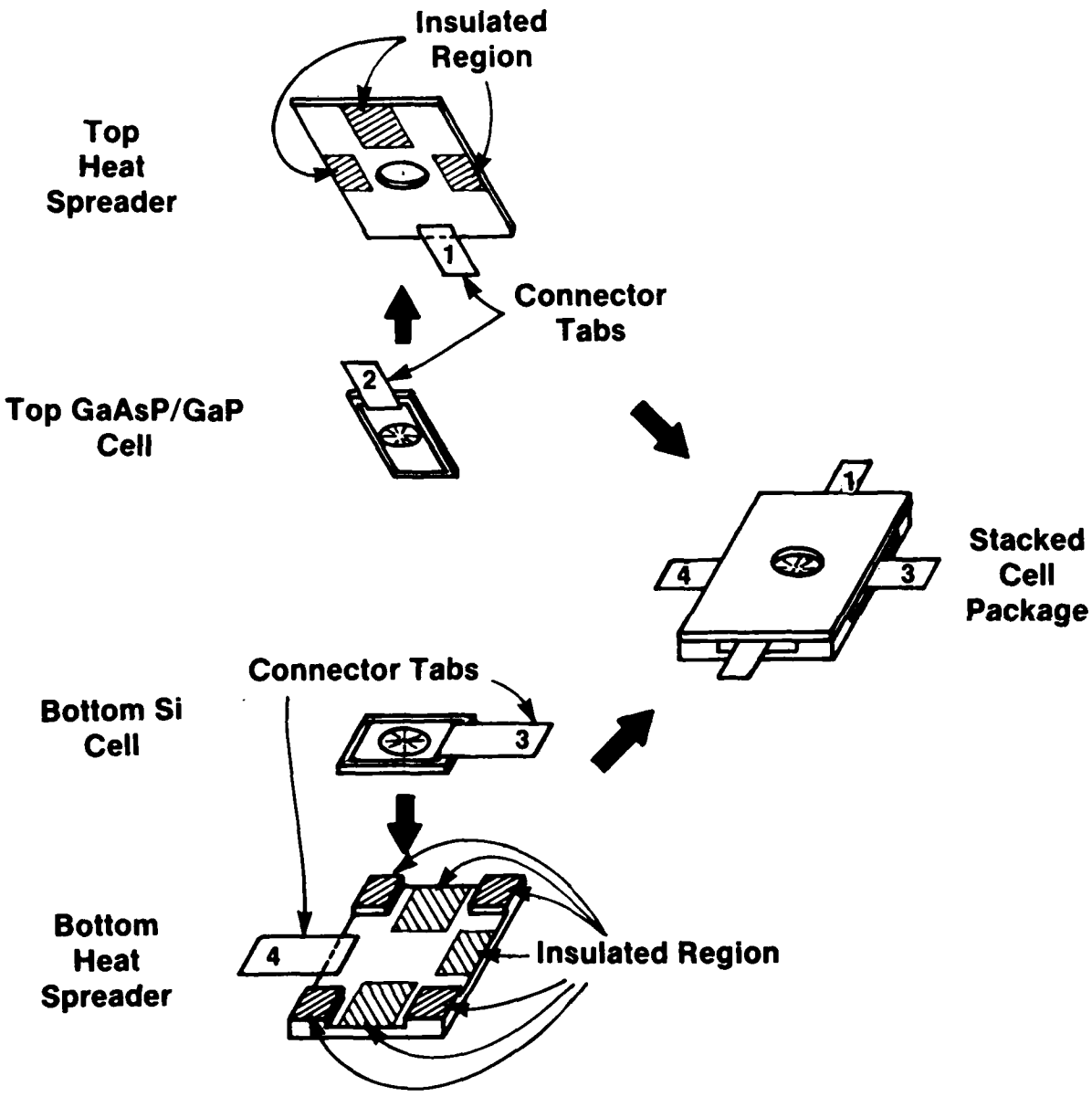


Figure 14 - A four-terminal cell package configuration that allows heat to be removed from the edges of the top device with a heat spreader.

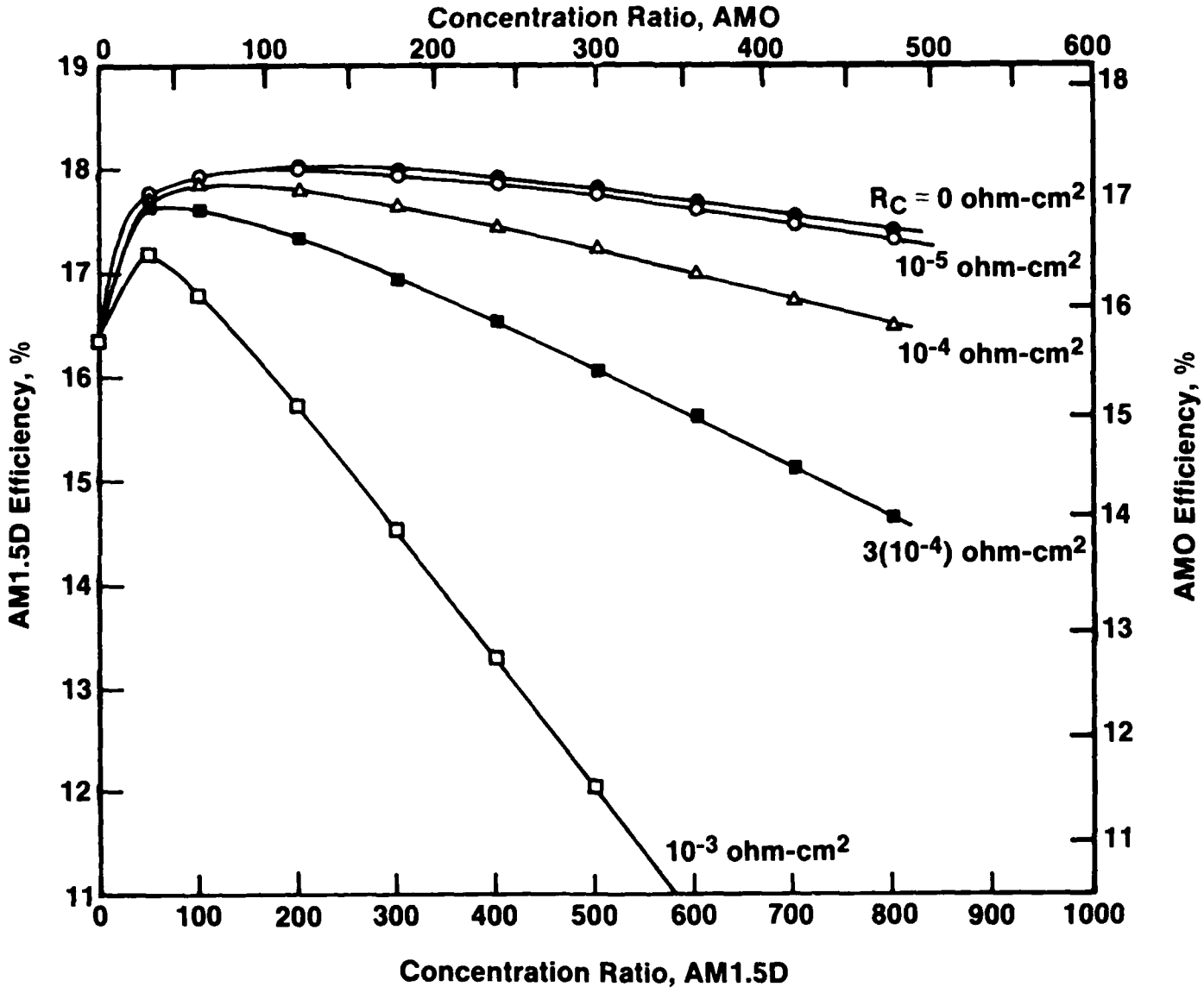


Figure 15 - The calculated dependence of the efficiency of the GaAsP on GaP device, on the sunlight concentration ratio for various values of specific contact resistance R_C to the grid metalization.

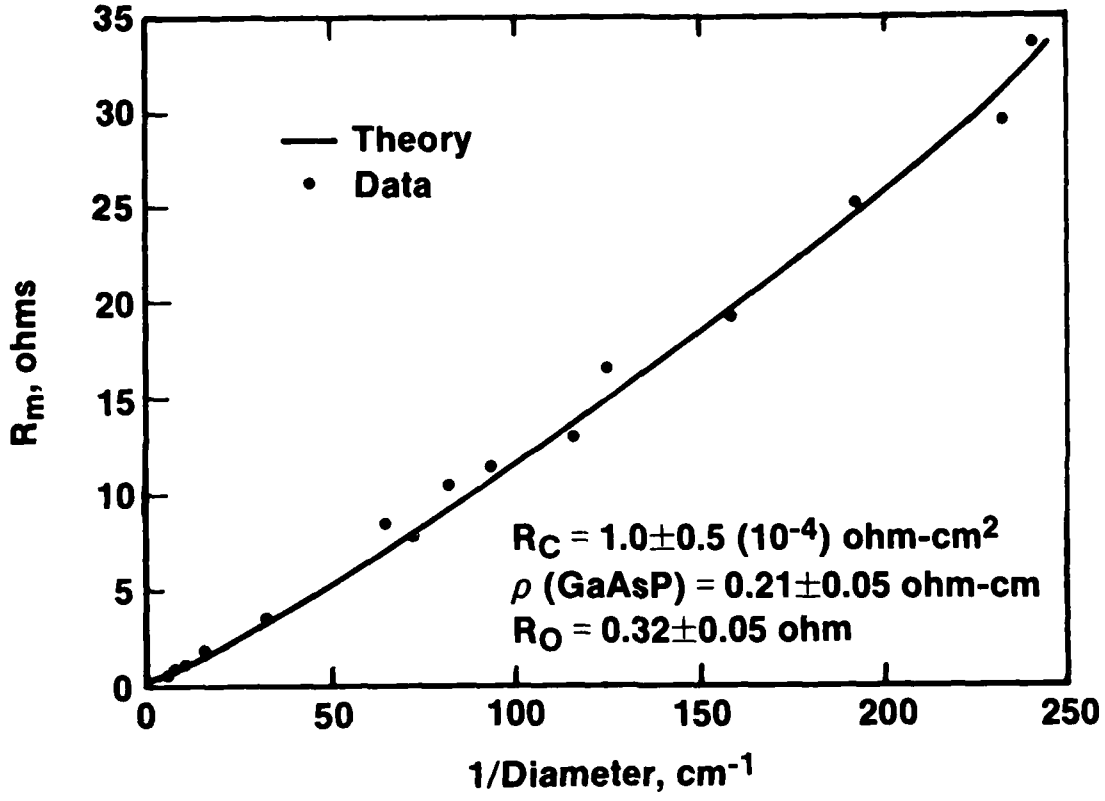


Figure 16 - The Cox and Strack analysis of measured data used to obtain specific contact resistance values.

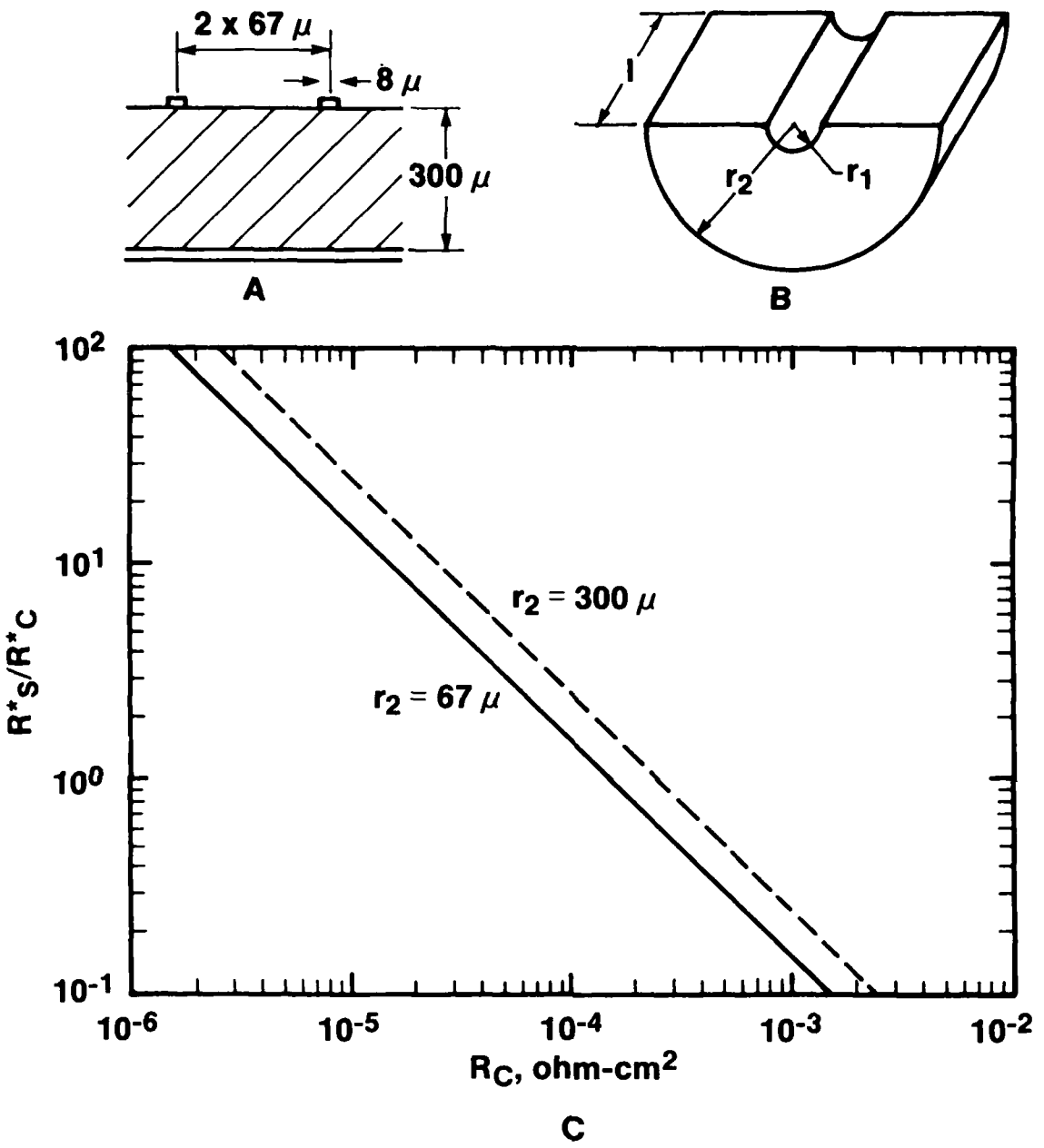


Figure 17 - The effect of spreading resistance of the bottom grid with: (A) showing the sample configuration, (B) showing the approximate theoretical model, and (C) giving the upper and lower bounds for the ratio of spreading-resistance to contact-resistance contribution to series resistance as a function of contact resistance.

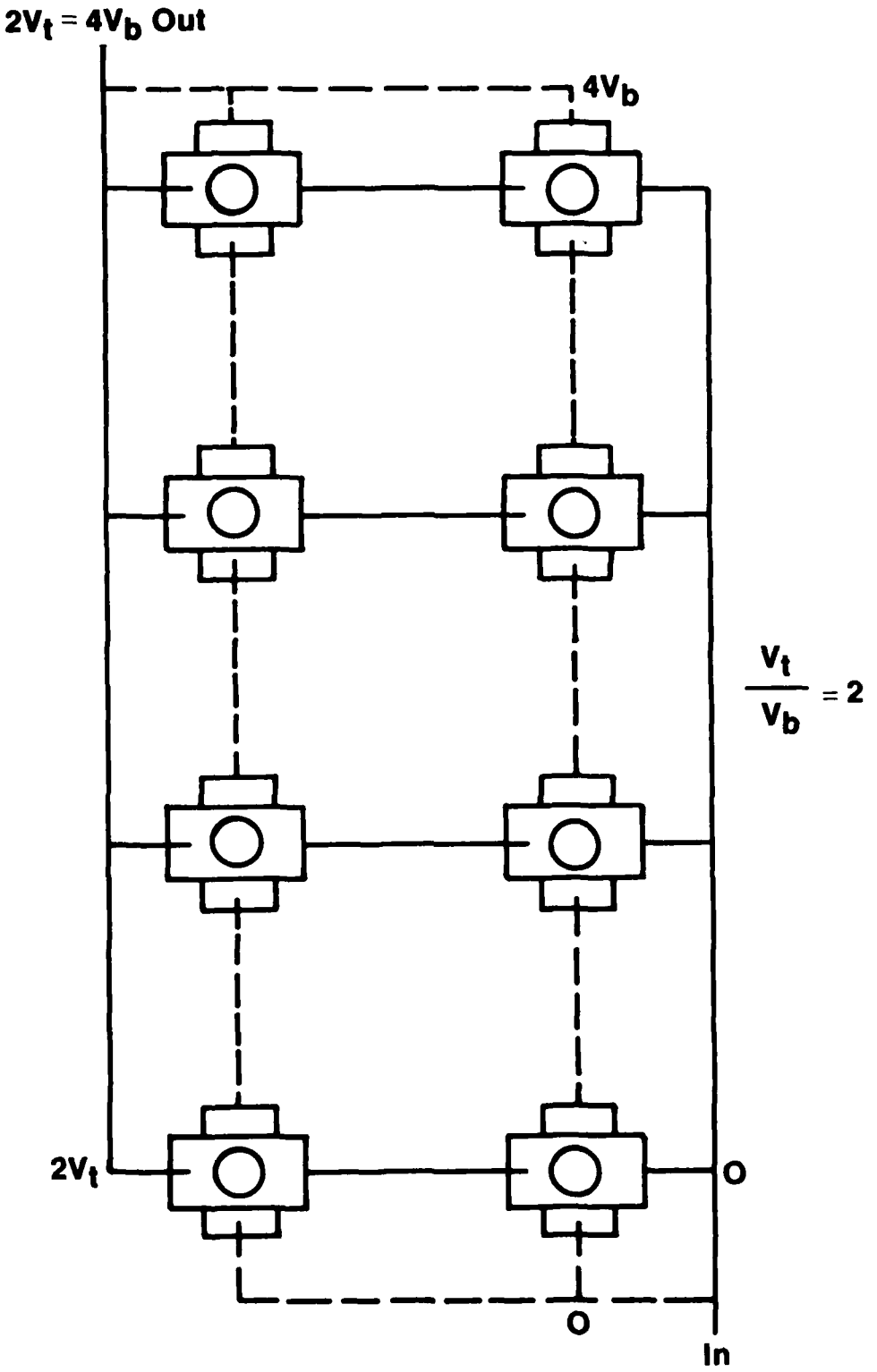


Figure 18 - A 2 x 4 wiring scheme for voltage matching four terminal stacked cells whose upper and lower voltages differ by a factor of 2.

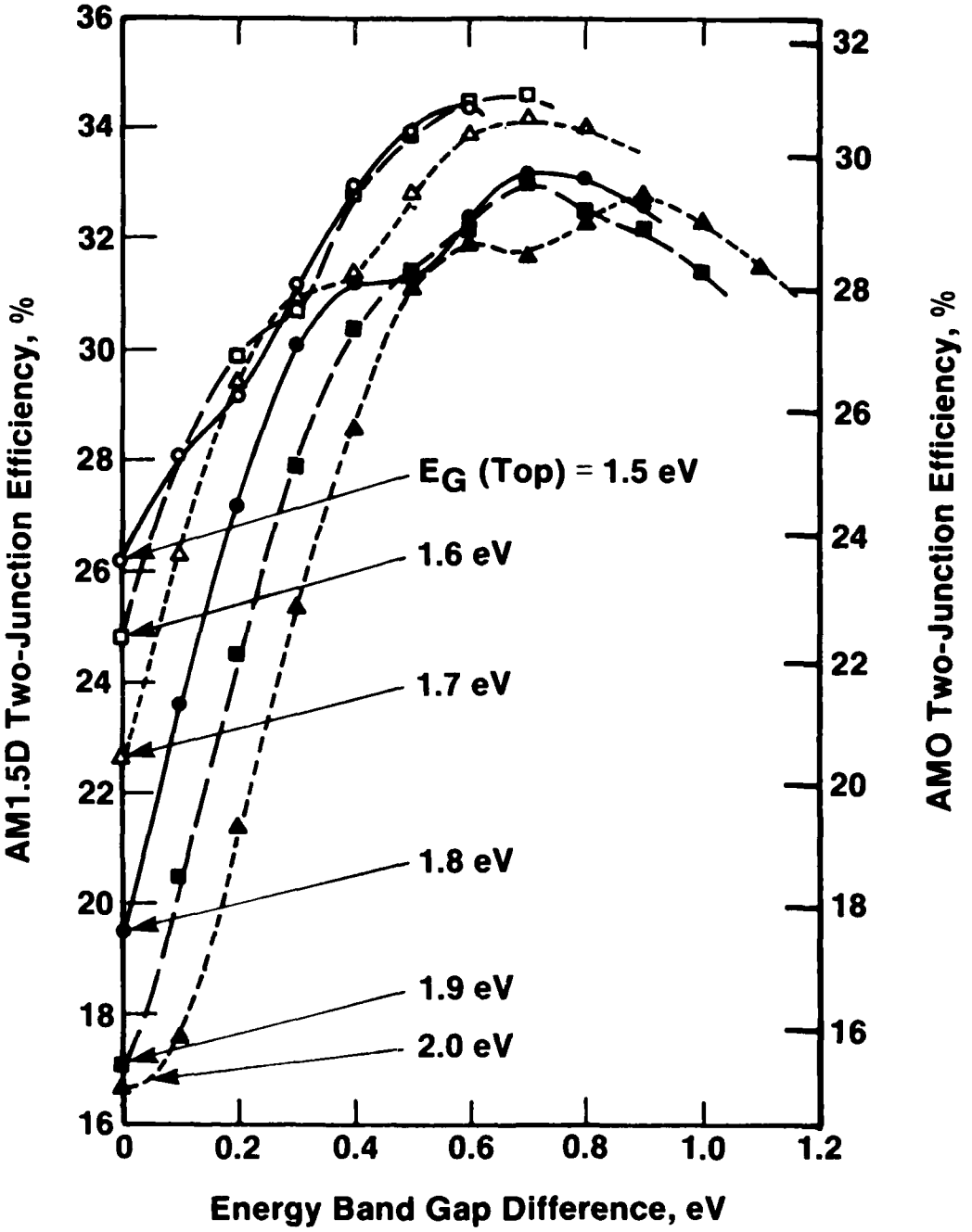


Figure 19 - The calculated, four-terminal, two-junction efficiency of stacked cells as a function of their energy band gap difference for various band gaps for the top junction E_G (Top). This is for a concentration ratio of 100x AM1.5D (approximately equivalent to 70x AMO).

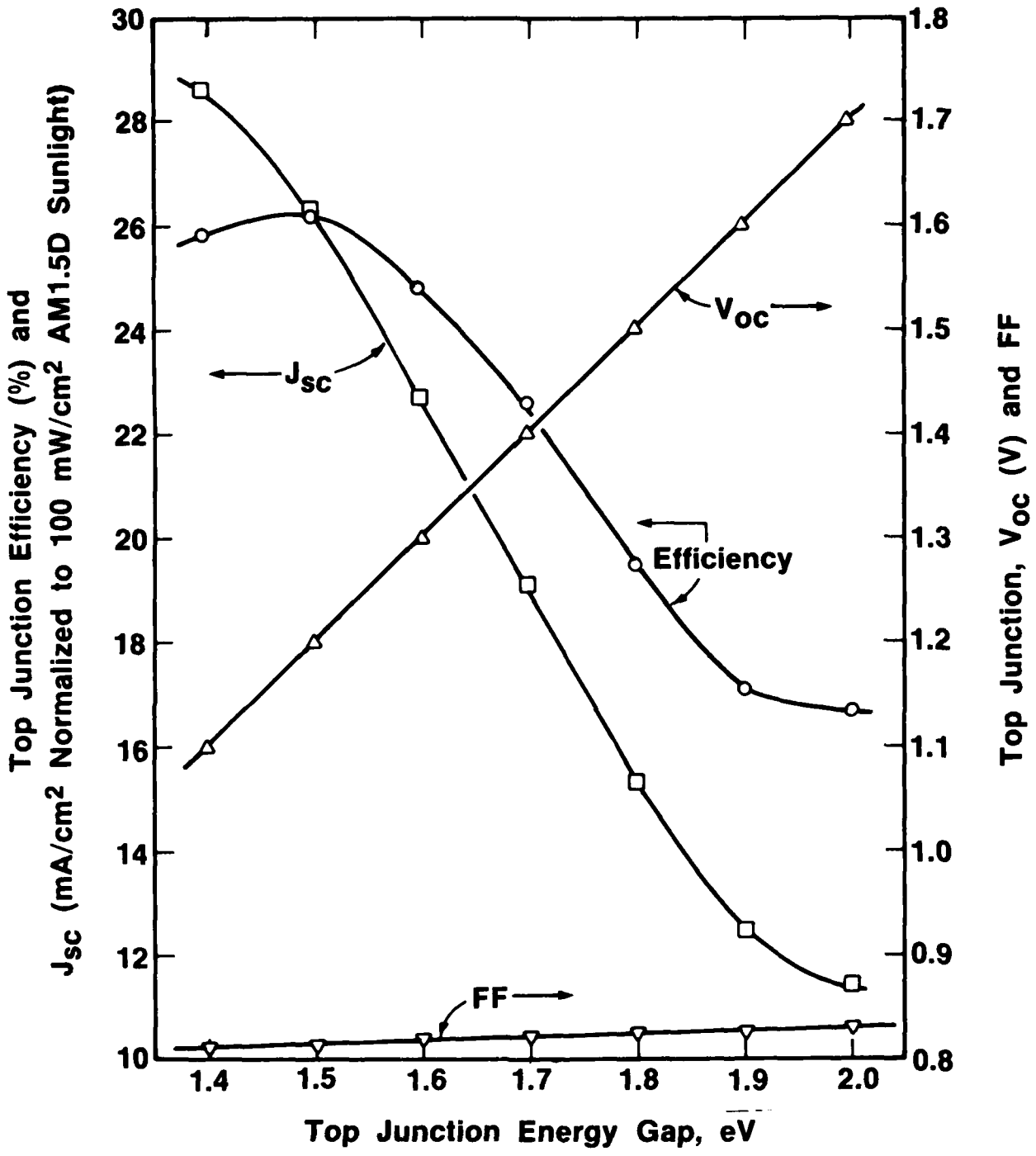


Figure 20 - The calculated performance of a top junction for stacked cells as a function of the top junction band gap E_G (Top) used to obtain the curves of Figure 19.

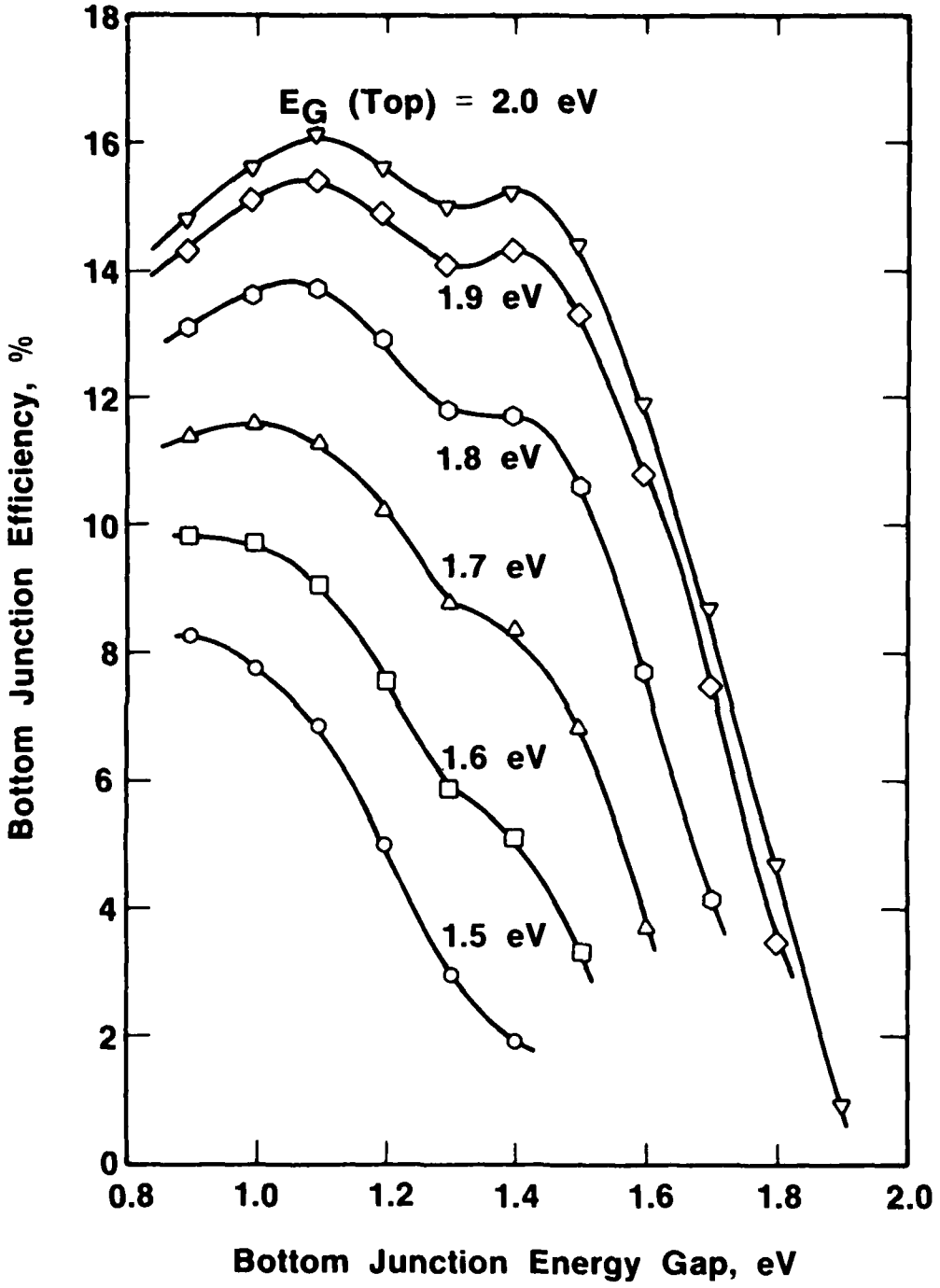


Figure 21 - The calculated efficiency of a bottom junction for stacked cells as a function of the bottom junction band gap for various top junction band gap values E_G (Top), used to obtain the curves of Figure 19.

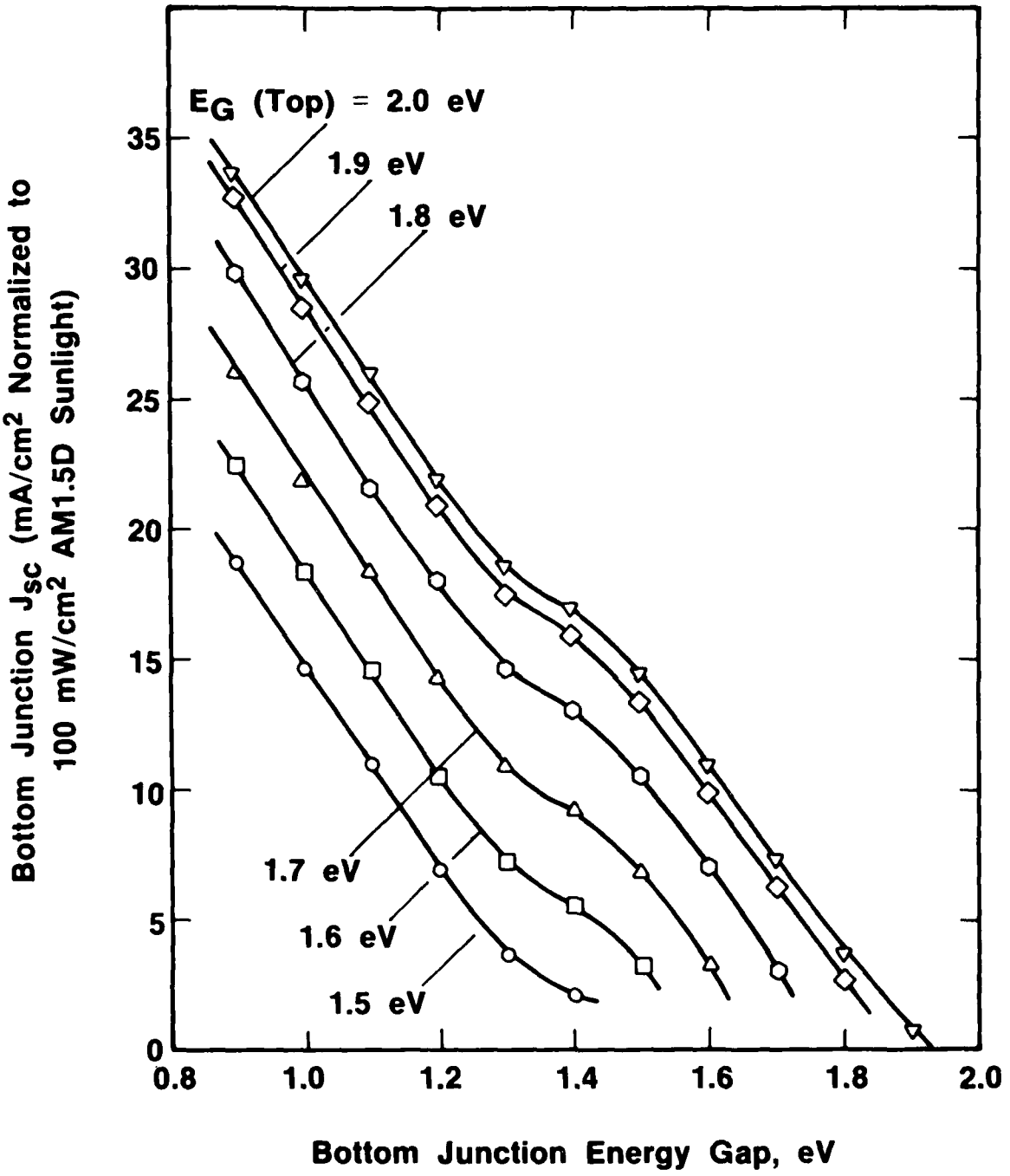


Figure 22 - The calculated bottom junction, short circuit current density J_{SC}, for stacked cells as a function of the bottom junction band gap for various top junction band gap values E_G (Top), used to obtain the curves of Figure 19.

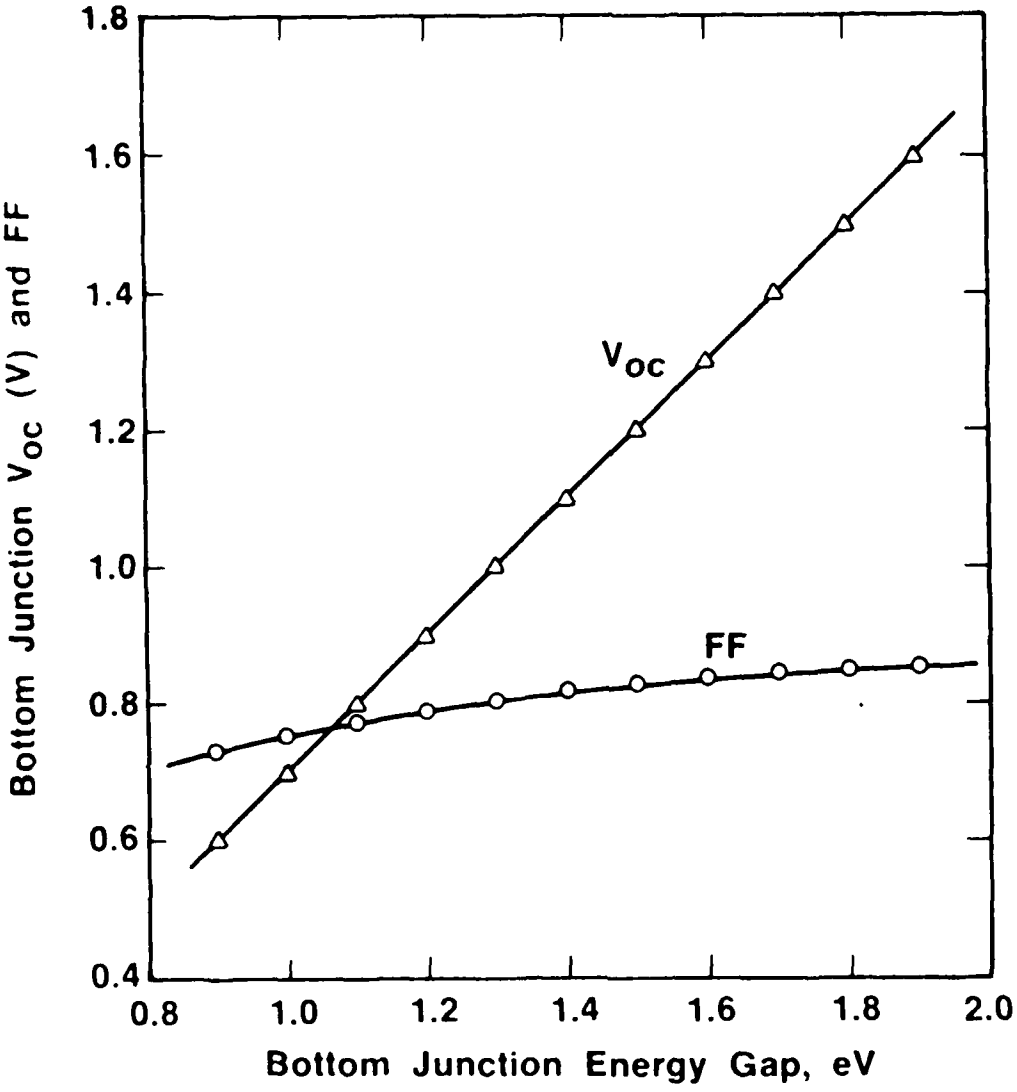


Figure 23 - THE CALCULATED OPEN CIRCUIT VOLTAGES AND FILL FACTORS FOR THE BOTTOM JUNCTION OF STACKED CELLS AS A FUNCTION OF THE BOTTOM JUNCTION BAND GAP USED TO OBTAIN THE FIGURE 19 CURVES

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